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Techniques for low power analog, digital and mixed signal CMOS integrated circuit design

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TECHNIQUES FOR LOW POWER ANALOG, DIGITAL AND MIXED SIGNAL CMOS INTEGRATED CIRCUIT DESIGN

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ABSTRACT

With the continuously expanding of market for portable devices such as wireless communication devices, portable computers, consumer electronics and implantable medical devices, low power is becoming increasingly important in integrated circuits. The low power design can increase operation time and/or utilize a smaller size and lighter-weight battery. In this dissertation, several low power complementary metal-oxide-semiconductor (CMOS) integrated circuit design techniques are investigated.

A metal-oxide-semiconductor field effect transistor (MOSFET) can be operated at a lower voltage by forward-biasing the source-substrate junction. This approach has been investigated in detail and used to designing an ultra-low power CMOS operational amplifier for operation at ± 0.4 V. The issue of CMOS latchup and noise has been investigated in detail because of the forward biasing of the substrates of MOSFETs in CMOS. With increasing forward body-bias, the leakage current increases significantly. Dynamic threshold MOSFET (DTMOS) technique is proposed to overcome the drawback which is inherent in a forward-biased MOSFET. By using the DTMOS method with the forward source-body biased MOSFET, two low-power low-voltage CMOS VLSI circuits that of a CMOS analog multiplexer and a Schmitt trigger circuits are designed. In this dissertation, an adaptive body-bias technique is proposed. Adaptive body-bias voltage is generated for several operational frequencies. Another issue, which the chip design community is facing, is the development of portable, cost effective and low power supply voltage. This dissertation proposes a new cost-effective DC/DC converter design in standard 1.5 μm n-well CMOS, which adopts a delay-line controller for voltage regulation.

CHAPTER 1

INTRODUCTION

With continuous expansion of market for portable light weight systems such as cellular phones, computers, consumer electronics items and implantable medical chips, low-power and thus, low-voltage design has become important in integrated circuits. The low-voltage/low-power design can increase operation time between battery recharging cycle and/or utilize a smaller size or a lighter-weight battery. Among several available technologies such as bipolar junction transistor (BJT), gallium arsenide (GaAs), complementary metal-oxide-semiconductor (CMOS), bipolar-CMOS (BiCMOS) [1-3], the CMOS technology has played a key and dominant role toward the development of low power portable devices for varied applications. For more than ten years, several low power CMOS design techniques have been investigated that include basic circuit design modification, architecture changes for implementing desired functions using low threshold voltage devices, power down strategies, optimization of transistor size, supply voltage scaling, along with other possible techniques [4-6]. In the following section, historic development and literature review on low-power CMOS design techniques are reviewed.

Low-power design drew attention beginning in 1990 with expansion in portable electronic market. An overview describing change in power dissipation of CMOS circuits changed since 1980 has been given by Kuroda and Sakurai [7]. Commercial digital signal processor (DSP) and microprocessor unit (MPU) were used as examples. Power dissipation of commercial CMOS circuits has increased since then due to increased clock frequency. For example, in 1982, power dissipation of a 5 V DSP chip was 0.1 W and

increased to 10 W in 1991. Power dissipation peaked in 1990-1991. After 1991, power dissipation of commercial CMOS chips have decreased due to increasing demand of large number of portable systems such as notebook computers and cellular phones where very low to ultra-low power dissipation is a primary requirement.

In 1996, Montanaro et al. [8] discussed typical power saving techniques related to a low power CMOS microprocessor design. They used a DEC Alpha 20164 CMOS microprocessor as a benchmark and reported power dissipation of 26 W at 200 MHz and 3.45 V supply voltage. Among several reported methods, method-1 reduces functions of a microprocessor (e.g. floating point function is removed for some special target applications). As a result, power dissipation is reduced by a factor of 3. Method-2 uses a processing scaling technique, which reduces node capacitances, and thus the power consumption. The power is reduced by a factor of 2 from 0.75 μm CMOS technology to 0.35 μm CMOS technology. In method-3, the capacitive load in the clock is reduced. The power is reduced by a factor of 3 after the latch circuits are redesigned. Method-4 reduces the clock rate from 200 MHz to 160 MHz, and the power dissipation is reduced by a factor of 1.25. Method-5 reduces the power supply voltage, V_{DD} from 3.45 V to 1.5 V. The power dissipation is reduced by a factor of 5.3. Among these methods, the voltage scaling technique is identified as a straightforward and also an aggressive technique due to dependence of power dissipation on the square of the supply voltage value. The power dissipation, P_{total} in digital CMOS circuits is summarized in the following relation [1]:

$$P_{total} = p_t \bullet (C_L \bullet V \bullet V_{DD}) \bullet f_{clk} + p_t \bullet (I_{SC} \bullet V_{DD} \bullet t_{switch}) \bullet f_{clk} + I_{leakage} \bullet V_{DD}. \qquad (1.1)$$

The first term in Eq. (1.1) is the switching part of the total power dissipation, where C_L is the equivalent load capacitance and f_{clk} is the clock frequency. V is the voltage swing and

p_t is the probability that a power dissipation transition occurs. The probability p_t is also called the activity factor and is normally taken to be unity. The voltage swing, V is same as voltage supply, V_{DD} except in pass-transistor based implementations where voltage swing is reduced by the threshold voltage [2]. The second term in Eq. (1.1) is characterized as a short-circuit power dissipation which is due to switching-on of both transistors (n-MOS and p-MOS transistors) in CMOS for a switching time, t_{switch} and characterized by the short circuit current, I_{SC}. The third term is Eq. (1.1) is due to subthreshold currents in MOSFETs and substrate injection effects. $I_{leakage}$ is the leakage current. The power-delay product or the energy per transition (P_{total}/f_{clk}) can be obtained from Eq. (1.1).

Neglecting short-circuit power dissipation part in comparison to the switching power, Eq. (1.1) reduces to the following equation which is normally used in CMOS design:

$$P_{total} = P_{dynamic} + P_{static} = C_L \bullet V^2{}_{DD} \bullet f_{clk} + I_{leakage} \bullet V_{DD} . \qquad (1.1a)$$

The first term in Eq. (1.1a) is characterized as the dynamic power dissipation, $P_{dynamic}$ and second term as the static power dissipation, P_{static}. It is inferred from Eq. (1.1a) that with scaling down of V_{DD}, dynamic power consumption is significantly reduced.

The 1997 International Technology Roadmap for Semiconductor (ITRS) report [10] showed a clear trend of decreasing the supply voltage in CMOS circuit design. The typical supply voltage of CMOS circuit was 5 V in 1980 and decreased to 2.5 V in 1997. It projected below 1 V operation for 2010. Low voltage CMOS design is a powerful and straightforward method to achieve low power dissipation.

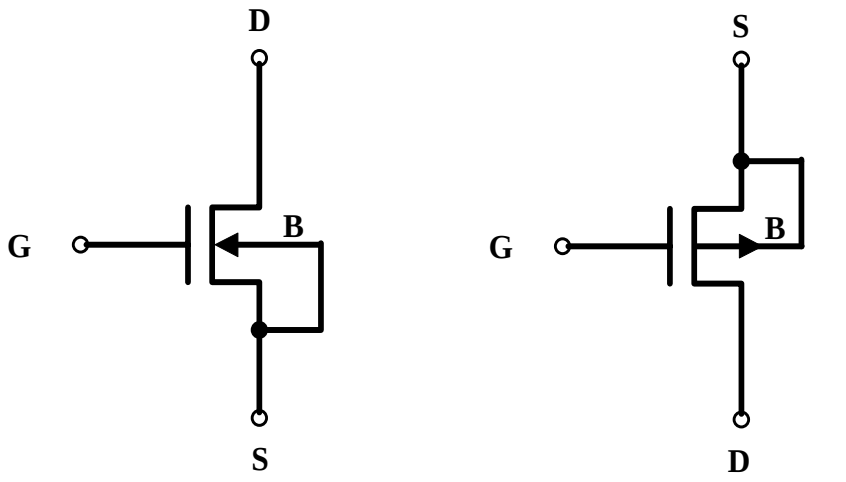
However, with low supply voltage, the voltage across gate and source of a MOS transistor drops. Thus, low threshold voltage MOSFETs are required for operation at a lower power supply voltage which requires a low threshold fabrication process. However, this increases the fabrication cost. Low threshold voltage transistors can be achieved utilizing present CMOS technologies by employing innovative circuit design techniques. Chen et al. [11] proposed the back gate forward body-bias method in 1996 to lower threshold voltage of a MOSFET in standard CMOS technology. Based on this method, inverter with power supply voltage < 1 V was designed. Another low power design using the forward body-bias is the dynamic threshold MOSFET (DTMOS) [12] technique where the body is tied to the gate. This method forces a forward body-bias when the transistor is on and a reverse body bias when the transistor is off. The DTMOS mode was demonstrated for a 0.6 V low power CMOS circuits. The forward body-bias method was used for the analog circuit design in 1998 by Blalock et al. [13]. A 1-V op-amp design in a standard digital CMOS technology was proposed. However, the bulk-driven op-amp design has disadvantages. The large bulk capacitance limits the frequency response and reduces the input impedance. The differential gain or the first stage gain of the op-amp is also reduced given the fact that the body-effect transconductance, g_{mb} is less than the gate transconductance, g_m. To overcome above disadvantages, a sub-1 V CMOS amplifier design using forward body-bias was presented by Lehmann and Cassia [14] in 2001. A 46-53 dB open loop gain is acquired under 0.8 V operation compared to 44 dB open loop gain obtained under 1-V operation of bulk-driven design. In this dissertation, a ± 0.4 V CMOS amplifier is designed using the forward body-bias method incorporating a level shift architecture which further lowers the power supply voltage requirement. A cascode

output stage increases the open-loop gain. Other low power techniques such as the modified DTMOS technique, adaptive bias generator and adaptive power supply voltage are also developed in this work. In the following section, a forward body-bias MOSFET method is described.

1.1 Forward Body-Bias Method

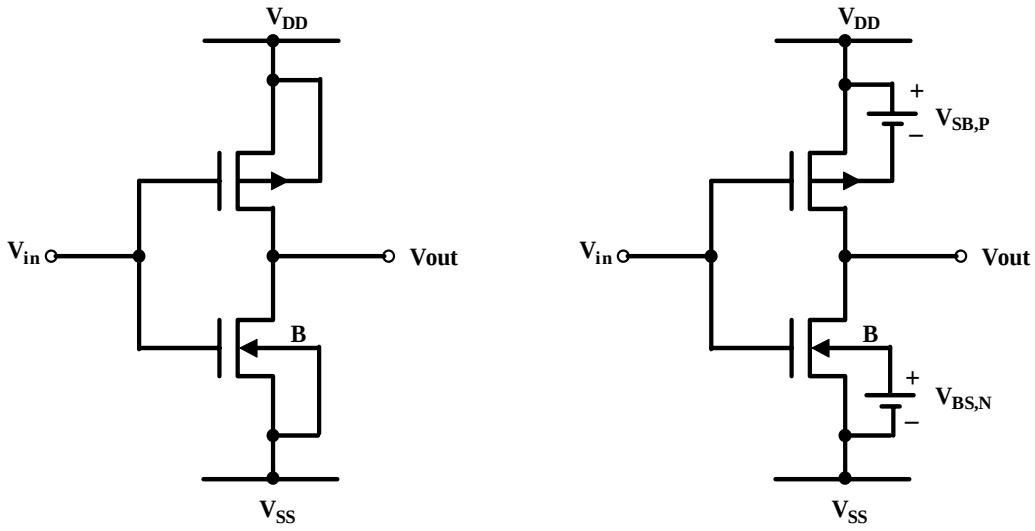
MOSFET is traditionally treated as a three-terminal device in a circuit design as shown in Fig. 1.1 where source and substrate terminal are shorted. It implies that the MOSFET operates as a zero-biased threshold device. On the other hand, a forward or reverse bias can be applied between the source and substrate of a MOSFET when used as a four-terminal device. Under the reverse body-bias, the MOSFET threshold voltage is increased. Under the forward body-bias, the MOSFET threshold voltage is reduced. The relationship between the threshold voltage and the body-bias is described in Chapter 2 in detail. Figure 1.2 (a) shows a standard CMOS inverter with shorted body-source transistors. Figure 1.2 (b) shows a CMOS inverter under forward body-bias conditions where the MOSFET is used as a four terminal device.

The back gate forward body-bias method shown in Fig. 1.2 (b) is compatible with CMOS processes. The threshold voltage of MOS transistors can be reduced electrically without any technology modification. In [13], MOS transistor has been used as a four-terminal device with drive-in voltage applied to the bulk or the substrate as shown in Fig. 1.3. In Fig. 1.3, a 1-V op-amp was designed using the bulk-drive technique, which provided an important solution to the threshold voltage limitation. A drawback of the bulk-driven technique is that it reduces the input impedance of an amplifier. Recently, the



(a) n-MOSFET **(b) p-MOSFET**

Figure 1.1: MOSFET as a three-terminal device (a) n-MOSFET (b) p-MOSFET. Here, S, G, D and B, respectively indicate source, gate, drain and substrate.



(a) Body-source shorted **(b) Forward-body bias**

Figure 1.2: CMOS inverter under (a) body-source short and (b) forward-body bias conditions. The $V_{BS,N}$ is the forward body-bias across the n-MOSFET and $V_{SB,P}$ is the forward body-bias across the p-MOSFET.

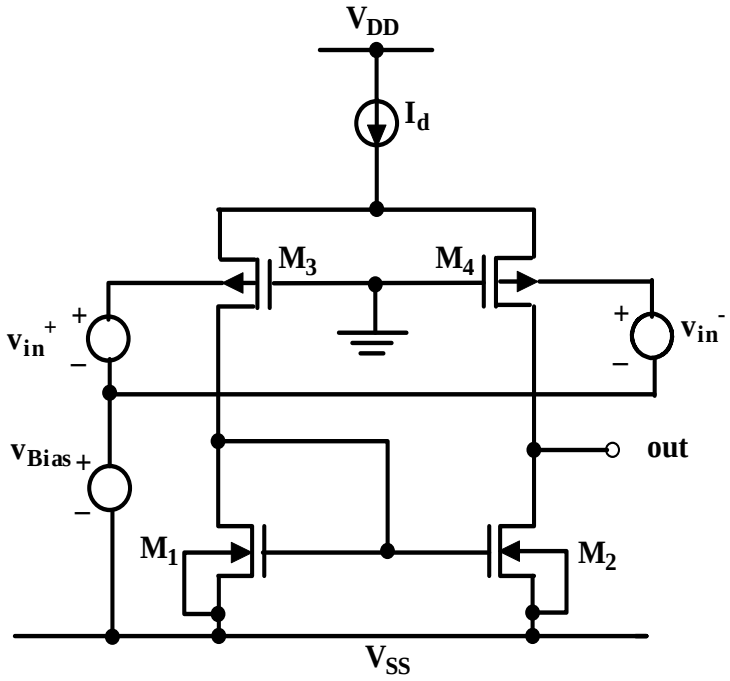


Figure 1.3: Circuit diagram of a bulk-driven CMOS amplifier.

back-gate forward bias technique has been used extensively to design low power digital and analog circuits [13-17].

In the following section, a major problem associated with amplifier-noise is introduced. A model is proposed for analysis and design of CMOS integrated circuits for digital and mixed-signal application.

1.2 Noise of Forward-Bias MOSFET

Noise is a major problem in amplifiers designed for low voltage applications. Flicker noise, thermal noise and shot noise are three types of noises associated with devices. Flicker noise also known as the 1/f noise is due to fluctuation in processing parameters and dominates at lower frequencies in a MOSFET. It is expressed as follows [18]:

$$\frac{\overline{v_{flicker}^2}}{\Delta f} = \alpha \frac{I_D}{g_m^2 f} \tag{1.2}$$

where $\overline{v_{flicker}^2}/\Delta f$ is the flicker noise voltage spectral density of the MOSFET, α is a constant for a given device. I_D is the drain current, *f* is the operational frequency and g_m is the device transconductance.

The thermal noise is caused by the random thermal motion of the electrons in the channel of a MOSFET. It is described by [18]

$$\frac{\overline{v_{thermal}^2}}{\Delta f} = \frac{8}{3} kT \frac{1}{g_m} \tag{1.3}$$

where $\overline{v_{thermal}^2}/\Delta f$ is the thermal noise voltage spectral density related to V_{gs} of the MOSFET in saturation, *k* is the Boltzman's constant, T is absolute temperature and g_m is

device transconductance. Thermal noise is inversely proportional to transconductance, g_m.

The shot noise is caused by the transport of carriers across the p-n junction. The transport is a random event since each carrier has a different energy and a velocity toward the junction. The shot noise in a diode is described by [18]

$$\frac{\overline{i_s^2}}{\Delta f} = 2qI_{DC} \tag{1.4}$$

where $\overline{i_s^2}/\Delta f$ is the shot noise current spectral density and is proportional to dc current, I_{DC} in a p-n junction.

Recently, 1/f noise has been reported in a forward body-biased MOSFETs [19]. A more complete analysis of noise associated with a forward body-biased MOSSFET is conducted in the dissertation. The noise models are developed for a forward body-biased MOSFET and used in the noise analysis of a 0.8 V forward body-biased CMOS operational amplifier design [20, 21].

In the following section, the dynamic threshold MOSFET (DTMOS) technique is described which is used in conjunction with the back gate forward-body bias method in designing low-power CMOS integrated circuits.

1.3 Dynamic Threshold MOSFET

The forward body-bias technique reduces the threshold voltage of a MOSFET. However, low threshold voltage increases the leakage current. In another method, gate is connected to the substrate [12] to obtain a dynamic threshold MOSFET (DTMOS). This method can be used in conjunction with the back-gate forward-bias method in designing low power CMOS circuits. Figure 1.4 shows a dynamic threshold MOSFET (DTMOS) inverter. This method lowers the threshold voltage when the transistor is turned on and

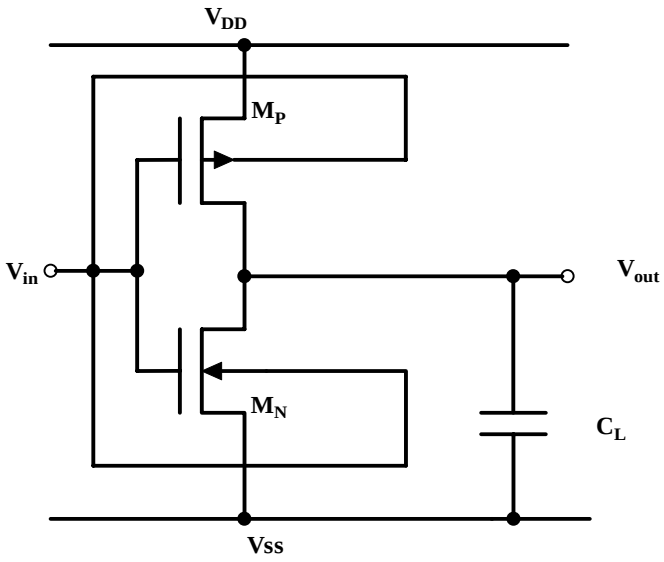


Figure 1.4: Circuit diagram of a DTMOS inverter.

increases the threshold voltage when the transistor is off. Thus, the method can reduce leakage current when the transistor is off.

In forward body-bias technique, forward body-bias should be limited to 0.4 V to avoid latchup of CMOS [2] which is due to turning-on of associated npn and pnp parasitic bipolar transistors. Figure 1.5 shows the vertical cross section of a CMOS inverter with parasitic bipolar junction transistors.

From Fig. 1.5, it is seen that the forward body-bias may turn on the p-n junction between the source and the substrate. In [15], it is reported that the forward body-bias limited to 0.4 V does not causes latchup. In DTMOS design, supply voltage is therefore limited to 0.4 V.

In the dissertation, we propose a modified DTMOS technique which can be operated at a low supply voltage. Using the modified DTMOS technique, following two practical circuits are designed: 1) a low voltage analog multiplexer and 2) a novel Schmitt circuits. The analog multiplexer, which can be used in an integrated sensor with readout circuits, preprocesses the signal from sensor to appropriate signal processing units such as an operational amplifier and analog-to-digital converter. Thus, the multiplexer plays an important role to select and transfer a signal from multi-channel inputs. Such circuits efficiently reduce power consumption and have a longer battery operation time. Integrating multiplexer and sensor on a chip will also reduce external noise, signal distortion and improve the system performance. In the dissertation, a 0.8 V low voltage, two-input analog multiplexer circuit is designed in a MOSIS 1.5 μm n-well CMOS technology [22]. The circuit consists of transmission gates as switches and an inverter. MOSFETs in the design of multiplexer use the dynamic body-bias method. The forward

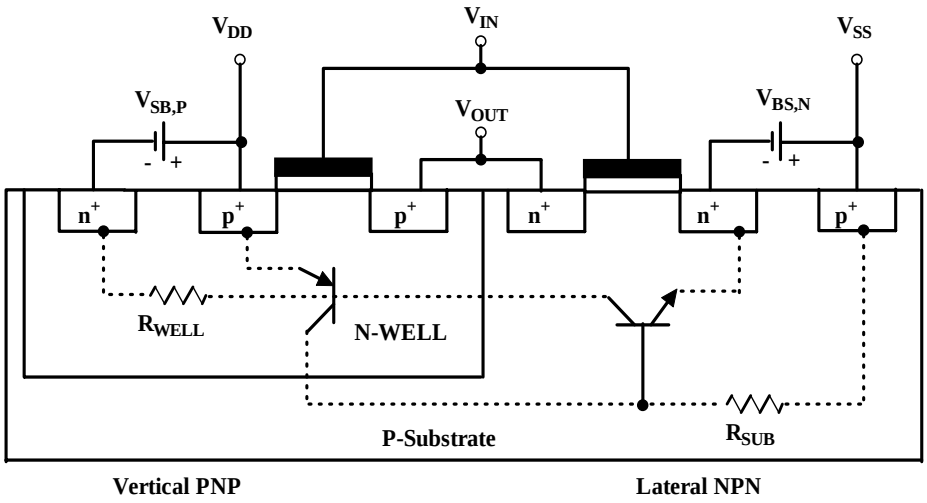


Figure 1.5: Cross section of a forward body-bias CMOS inverter including parasitic bipolar transistors.

body bias is limited to no more than 0.4 V to avoid CMOS latchup. The reverse body bias is limited to 0.4 V and allows the MOSFET to turn-off fully and suppresses the subthreshold leakage. The improved dynamic threshold MOSFET inverter achieves low voltage operation and reduces signal leakage. The on-to-leakage ratio of the DTMOS transmission gate is 120 dB.

Another novel digital circuit (Schmitt trigger) is designed using the DTMOS technique where only four transistors are used. Schmitt triggers are widely used for waveform shaping under noisy conditions in electronic circuits. In VLSI circuits, they are often used at the chip input side and as single-ended receivers in DRAMs. Low power novel Schmitt trigger circuits have been designed in MOSIS 1.5 μm n-well CMOS and experimentally tested for operation at 1 V and 0.4 V [23]. The method exploits lowering of the threshold voltage of a MOSFET under a forward-biased substrate. Dynamic body-bias method is incorporated in a feed-back loop. This combination of two methods has significantly reduced the operational voltage and thus the power dissipation.

1.4 Adaptive Body-Bias Generator

In some digital circuits such as microprocessors, various modules or sub-circuits are not necessarily required to operate under a fixed clock. Some of the modules or sub-circuits may be in standby or operating at a low performance level, while the other modules or sub-circuits may keep working at their highest performance level. Furthermore, modules may work at different clock frequencies. When operation or the switching frequency is high, low threshold voltage is needed. When operation or the switching frequency is low, a high threshold voltage is helpful to reduce the total leakage current. In such a circuit, varying body-bias can achieve optimized performance and

power consumption. Thus, an adaptive body-bias generator is highly desirable to vary the body-bias of a CMOS circuit. In this work, a simple adaptive body-bias technique is proposed. Adaptive body-bias voltage is generated for various operational frequencies. When operational frequency decreases, body-bias voltage is switched from a forward body-bias to a reverse body-bias.

1.5 Dynamic Voltage Scaling

Dynamic voltage scaling (DVS) has proved to be an effective low-power design technique in modern digital systems. In a DVS technique, a higher supply voltage is applied when a digital integrated circuit (IC) is running at a high speed and a lower supply voltage is applied when a digital IC is not in its peak performance such as non-critical path or standby mode. In a DVS technique, a smart power supply generator is essential which generates adaptive supply voltage according to operational frequency. Thus, another important issue, which the chip design community is facing, is the development of a portable, cost effective power supply. DC/DC converter is found to be the best solution in adaptive supply voltage generation [24-27]. A basic architecture of DC/DC converter is shown in Figure 1.6.

In Fig. 1.6, S_1 and S_2 are switches. L and C are inductor and capacitor, respectively which consist of a lossless low pass filter to achieve a small output ripple. Vg is power supply voltage and Vout is output voltage. When S_1 is 'on' and S_2 is 'off', the capacitor, C is charged. Charging current is given as

$$I = \frac{V_g - V_{out}}{L} T_1 \tag{1.5}$$

where T_1 is the time when S_1 is 'on'.

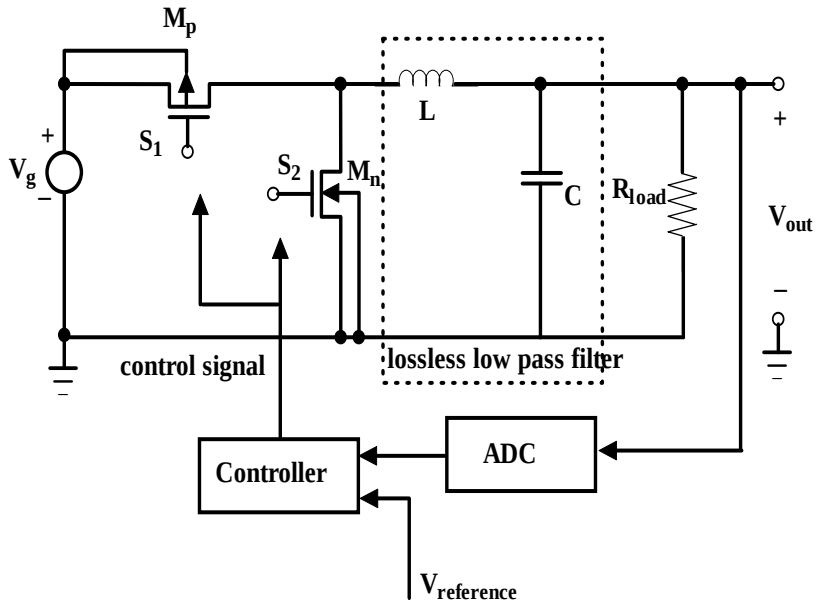


Figure 1.6: Basic architecture of a DC/DC converter.

When S_2 is 'on' and S_1 is 'off', the capacitor, C is discharged. Discharging current is given by

$$I = \frac{V_{out}}{L} T_2 \tag{1.6}$$

where T_2 is the time when S_2 is 'on'.

The output voltage is determined by the duty cycle of the control signal which is generated by the controller. Recently digitally controlled DC/DC converter has drawn a good attention due to its fast response, low power consumption and compatibility with standard digital CMOS processes [25]. Several existing implementations of digital controller need high-resolution, high-speed analog-to-digital (A/D) converter, which occupies a large chip area and consumes significant power. The A/D converter samples and converts the regulated output voltage into digital signals in a feedback loop to determine the duty cycle of the control signal and thus the output voltage of DC/DC converter. Its bandwidth limits the overall dynamic response of the power converter. The delay-line based controllers reported in [26, 27] transform a voltage signal into a frequency signal, and use digital signal processing circuits for the voltage regulation. Power consumption of delay-line can be much lower than A/D converter implementations.

For improved performance and better control, a pulse-train technique is proposed in reference [28]. By adopting a pulse train instead of a fixed pulse as a gate control signal of switches, the converter successfully avoids over-charging or discharging of the capacitor through the inductor during transition. The output ripple voltage is reduced. However, the pulse-train technique slows down the transient response since the converter takes a longer time to deliver the energy to the load. In this dissertation, an adaptive

pulse-train technique [29] is proposed and implemented which is incorporated in delay-line controller for the low ripple and fast transient response. An internal control signal can enable pulse-train function for high-resolution regulation in steady mode and disable it for the fast dynamic response in the transient mode.

1.6 Goals and Objectives

In the following chapters, the low power methodology, circuit design, simulation results, post-layout measurements and experimental results are discussed.

Chapter 2 explains the forward body-bias method for low-voltage operation. A basic model of a forward body-biased MOSFET is derived. A CMOS amplifier, which incorporates the forward body-bias method and level shift current mirror, is designed. The amplifier is designed in 1.5 μm n-well CMOS technology. Experimental results are presented and compared with the corresponding simulated values.

Chapter 3 proposes a noise model for a forward body-bias MOSFET and an amplifier. The simulation results for the noise analysis using the proposed noise model are also described.

Chapter 4 explains the concept of dynamic threshold MOSFET (DTMOS). An improved DTMOS multiplexer is designed, which consists of a DTMOS inverter and switches. The mechanism of DTMOS is used in a feedback loop in a low voltage Schmitt trigger circuit design. Experimental results are presented.

Chapter 5 proposes a CMOS body-bias generating circuit designed for generating adaptive body-biases for MOSFETs in CMOS circuits for low voltage operation**.** The frequency adaptive body-bias generator circuit has been implemented in 1.5 μm n-well

CMOS technology. A close agreement is obtained between the simulated output characteristics and corresponding experimentally measured behavior.

Chapter 6 describes another important low power issue - an adaptive voltage scaling method. An adaptive DC/DC converter is designed to generate a frequency adaptive supply voltage.

Chapter 7 provides a summary of the work presented and scope for future work.

Appendix A presents the MOSIS level 3 MOS model parameters [30] used in CMOS circuit simulations using SPICE.

Appendix B summarizes the MOSFET modeling, from the measured I-V characteristics. The extracted model parameters are compared with the corresponding parameters obtained through MOSIS.

Appendix C summarizes measurement techniques used in the characterization of the low power CMOS amplifier.

Appendix D gives the list of publications.

CHAPTER 2*

FORWARD BODY-BIAS TECHNIQUE

In low power design, voltage scaling is a straightforward technique and becomes more effective due to the power consumption's square relation with the supply voltage. However, with low supply voltage, the voltage across the gate and the source of a MOS transistor drops. Thus, low threshold MOSFETs are needed for operation at the low power supply voltage. To obtain low threshold voltage transistors utilizing current CMOS technologies, circuit design techniques must be developed that lower device threshold values. In this chapter, forward body-bias technique is used for designing a low power and low voltage operational amplifier. Before introducing the methodology, threshold voltage of MOS transistor, which is the basis of the forward body-bias technique for reducing the threshold voltage, is described.

2.1 Threshold Voltage of the MOSFET

Threshold voltage modeling is described in detail in [1, 31]. The basic steps are summarized in this section for completeness. Figure 2.1 shows a long-channel enhancement mode n-MOSFET where body, source and drain terminals are grounded. A voltage, V_{GS} is applied to the gate and initially it is zero. As the gate voltage is increased from a zero value to a positive magnitude, initially a depletion region is created followed by weak inversion region close to the S_i-S_iO_2 interface. As the gate voltage is further increased, a condition of strong inversion sets in where a p-type silicon is inverted to an

* Part of this work is reported in following publications:
1. C. Zhang, A. Srivastava and P. K. Ajmera, "A 0.8 V ultra-low power operational amplifier design," *Proc. of 45th IEEE International Midwest Symposium on Circuits and Systems*, Vol. 1, pp. I 9-12, 2002.
2. C. Zhang, T. Xin, A. Srivastava and P. K. Ajmera, "Ultra low-power CMOS operational amplifier for a neural microprobe," *Proc. of SPIE*, Vol. 5005, pp. 29-35, 2003.
3. T. Xin, P. K. Ajmera, C. Zhang and A. Srivastava "High-aspect ratio neutal probes for monolithic integration with ultra-low power CMOS operational amplifier circuit," *Proc. of SPIE*, Vol. 5389, pp. 20-25, 2004.

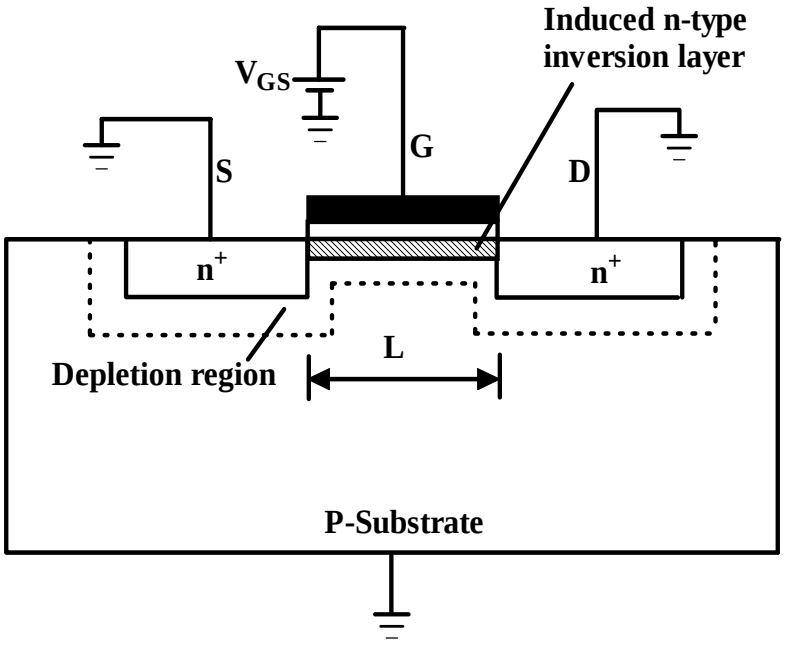


Figure 2.1: The cross-section of an n-MOS with positive gate voltage applied showing the depletion region and the inversion layer [1]. G is gate, D is drain and S is source.

n-type silicon. This condition occurs at a certain value of the gate to source voltage and is called the threshold voltage, V_T.

These are three voltage components which contribute to the threshold voltage, V_T of a MOSFET. These voltage components are the gate to semiconductor work function difference (ϕ_{GC}), $-Q_{OX}/C_{OX}$ due to fixed oxide charge present in the oxide and at the S_i-S_iO_2 interface, and a gate voltage ($-2\,\phi_F - Q_B/C_{OX}$) to change the surface potential to the strong inversion condition and to offset the induced depletion region charge, Q_B. ϕ_F is Fermi energy and C_{OX} is the gate oxide capacitance per unit area. Mathematically, V_T can be expressed as follows:

$$V_T = \phi_{GC} - \frac{Q_{OX}}{C_{OX}} + (-2\phi_F - \frac{Q_B}{C_{OX}}) . \tag{2.1}$$

The first part $(\phi_{GC} - \frac{Q_{OX}}{C_{OX}})$ represents voltage required to establish flat-band (FB) condition. The second part $(-2\phi_F - \frac{Q_B}{C_{OX}})$ represents voltage required to bend the bands in Si through a potential of $2\phi_F$.

The voltage required to establish the FB-condition is described by

$$V_{FB} = \phi_{GC} - \frac{Q_{OX}}{C_{OX}} . \tag{2.2}$$

For n-MOSFET, the charge in the depletion region per unit area, Q_B is given by

$$Q_B = qN_A X_d = -\sqrt{2qN_A\varepsilon_{Si} \mid \phi_s - \phi_F \mid} \ \text{ for } \mid \phi_s - \phi_F \mid \geq 0 \tag{2.3}$$

where N_A is the substrate doping density, X_d is thickness of the depletion region and ε_{Si} is the permittivity of silicon. The electrostatic potential at the silicon surface with

respect to Si bulk is described by ϕ_S. At the condition of strong inversion, with no body bias ($V_{SB} = 0$), the depletion region charge, Q_{BO} is given by

$$Q_{BO} = -\sqrt{2qN_A\varepsilon_{Si} \mid -2\phi_F \mid} \quad . \tag{2.4}$$

In presence of a body bias ($V_{SB} \neq 0$), the surface potential required to produce the inversion region is modified to $\mid -2\phi_F + V_{SB} \mid$. The corresponding charge stored in the depletion region, Q_B is given by

$$Q_B = -\sqrt{2qN_A\varepsilon_{Si} \mid -2\phi_F + V_{SB} \mid} \quad . \tag{2.5}$$

For the n-MOSFET, Eq. (2.1) can be written as

$$V_T = \phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} - \frac{Q_B - Q_{BO}}{C_{OX}} \text{ , or} \tag{2.6}$$

$$V_{TN} = V_{TNO} + \gamma(\sqrt{\mid 2\phi_F + V_{SB} \mid} - \sqrt{\mid 2\phi_F \mid}) \tag{2.7}$$

where V_{TN} is the threshold voltage of n-MOSFET and V_{TNO} is the zero-bias threshold voltage with $V_{SB} = 0$. The parameters, γ is called the body-effect coefficient or body factor and is given by $\gamma = \frac{1}{C_{OX}}\sqrt{2q\varepsilon_{si}N_A}$.

Normally, $V_{SB} \leq 0$, results in $V_T \geq V_{TO}$. With the substrate bias, $V_{SB} \geq 0$, V_T is less than V_{TO}. Thus, an n-MOSFET can be designed to operate at a reduced voltage. Equation (2.7) can be used for the p-MOSFET with the use of proper sign [1]. The threshold voltage of a p-MOSFET, V_{TP} is given by

$$V_{TP} = V_{TPO} - \gamma(\sqrt{\mid 2\phi_F + V_{SB} \mid} - \sqrt{\mid 2\phi_F \mid}) . \tag{2.8}$$

where V_{TPO} is the zero biased threshold voltage of n-MOSFET, $\gamma = \frac{1}{C_{OX}}\sqrt{2q\varepsilon_{si}N_D}$ and N_D is the doping density in n-substrate.

2.2 Forward Body-Bias

With the proliferation of battery-powered applications, low power circuit design is extremely desirable for portable devices such as cellular phones, hand-held computers and personal assistant devices. Reducing power supply voltage is a straightforward method to achieve low power consumption. Forward body-bias technique is very useful in the low voltage CMOS circuits design. In reference [11], a low voltage inverter is designed by this technique. Forward body bias MOSFETs are used in a 0.8 V CMOS amplifier design and reported in reference [16]. Forward body-bias technique is also used in dual threshold voltage technique without requiring complex dual threshold fabrication technology [12].

However, there is a limit to the amount of V_{SB}, which can be applied since large V_{SB} may trigger CMOS latchup. In an earlier work, it has been reported that latchup action will not be triggered in CMOS circuits for source-substrate forward-biased voltage less than 0.4 V [15]. The latchup in CMOS has been investigated for the present design and biasing conditions. Figure 2.2 shows the vertical cross section of an n-well CMOS with parasitic *npn* and *pnp* bipolar junction transistors. The corresponding equivalent circuit including parasitic *npn* and *pnp* bipolar junction transistors is shown in Figure 2.3 where source-substrate junctions are forward-biased and V_{DD} is 0.8 V. Figure 2.4 shows the simulated latchup current versus the forward body-bias voltage. It is seen from Fig. 2.4 that the latchup action does not take place for the substrate-bias up to 0.4 V. Figure 2.5 shows the current between source and substrate junction due to varying forward-

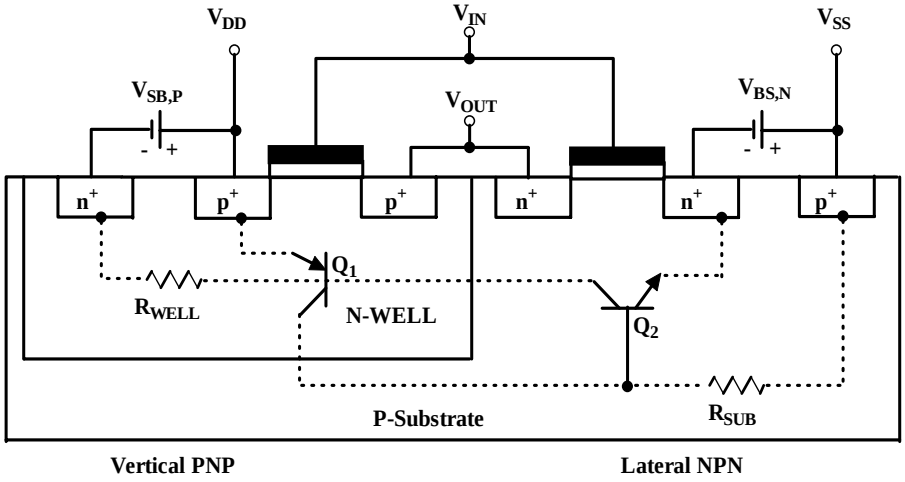


Figure 2.2: Vertical cross-section of an n-well CMOS showing parasitic bipolar junction transistors. Same as Fig. 1.5 but redrawn here for convince.

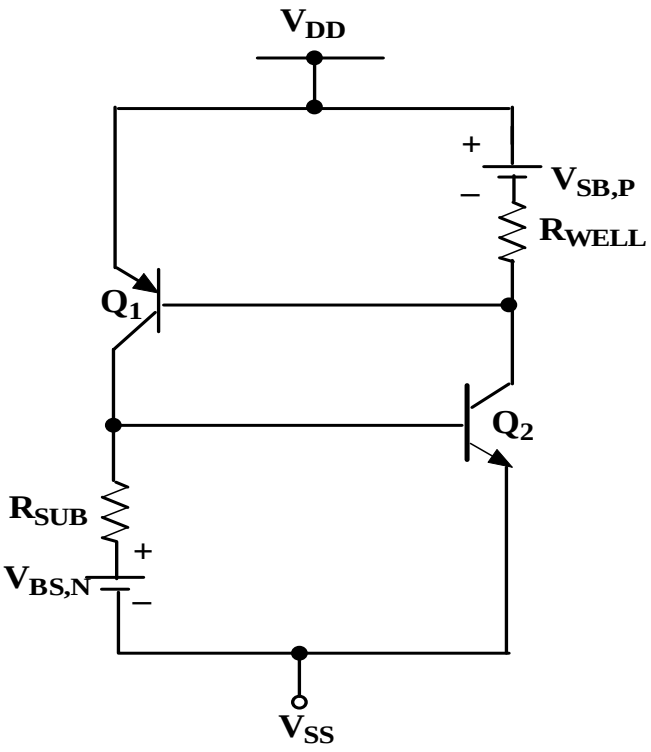


Figure 2.3: Extracted equivalent circuit of Figure 2.2.

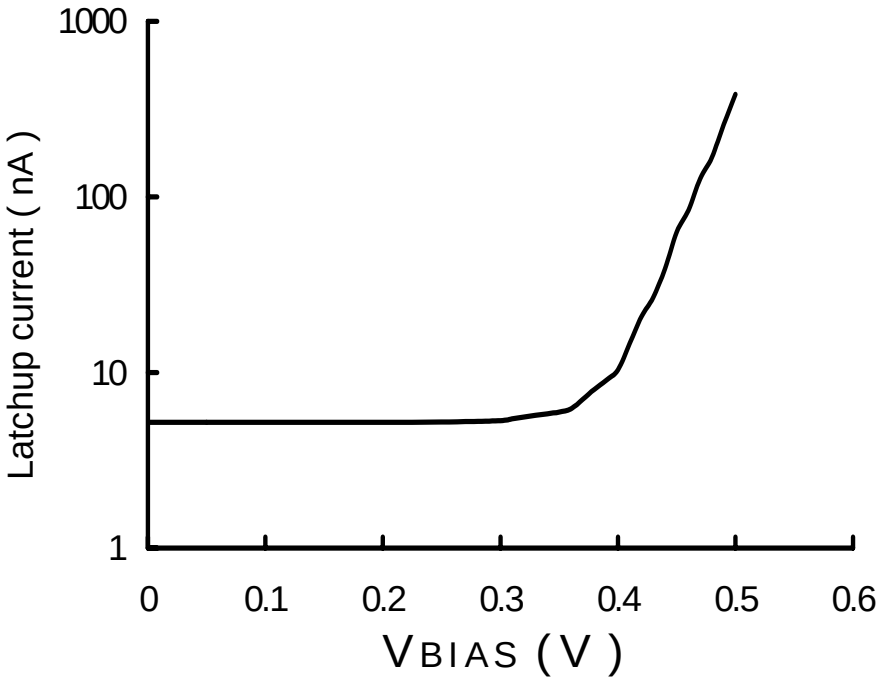


Figure 2.4: Latchup current under forward biased source-substrate condition for V_{DD} = 0.4 V and V_{SS} = -0.4V.

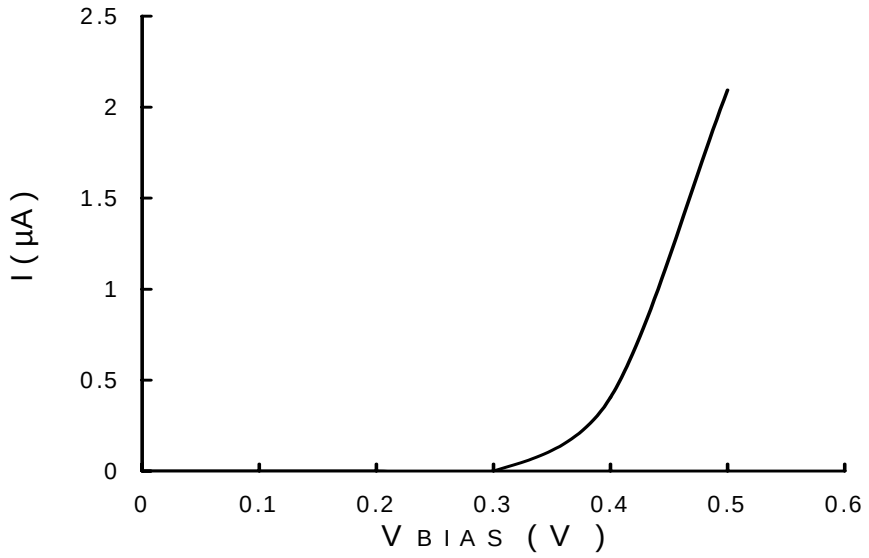


Figure 2.5: Current through forward biased source-substrate junction in an n-MOSFET.

biased substrate in a typical n-MOSFET. The source-substrate n^+-p junction area is 4.8 μm x 3.2 μm. It shows that the current in a forward biased source-substrate n^+-p junction is negligible when the junction is biased below 0.4 V. Figure 2.6 shows the reduction of threshold voltages with increasing forward body bias in fabricated n- and p-MOSFETs in a standard 1.5 μm n-well CMOS process. The dotted lines in Figure 2.6 show the calculated threshold voltage using Eq. (2.7). The measured threshold voltages are shown by the solid lines.

2.3 Amplifier Design Using Forward Body-Bias Technique

Amplifiers are the basic and widely used circuits in CMOS analog and mixed-signal systems. In the past, work has been reported on low-voltage CMOS amplifier designs wherein, bulk driven and current driven have been used [13, 14, 32]. In the bulk driven case, the input is directly connected to the substrate and not the gate of the MOSFET. In the current driven case, the substrate-source junction is forward biased by a bias current through another MOSFET connected to the substrate. Recently, we have reported a 0.8 V low power CMOS amplifier design using forward body-biased MOSFETs [16].

2.3.1 A Two-Stage CMOS Amplifier Topology

Figure 2.7 shows the circuit diagram of a two-stage CMOS amplifier. The first stage in Fig. 2.7 consists of a p-channel differential pair, M_1-M_2 with an n-channel current mirror load, M_3-M_4. Transistor, M_7 provides the bias current for the first stage. The second stage consists of an n-channel level shift amplifier, M_9 with a p-channel current-source load, M_8. Transistors, M_5 and M_6 provide the bias current and C_C is pole splitting capacitor.

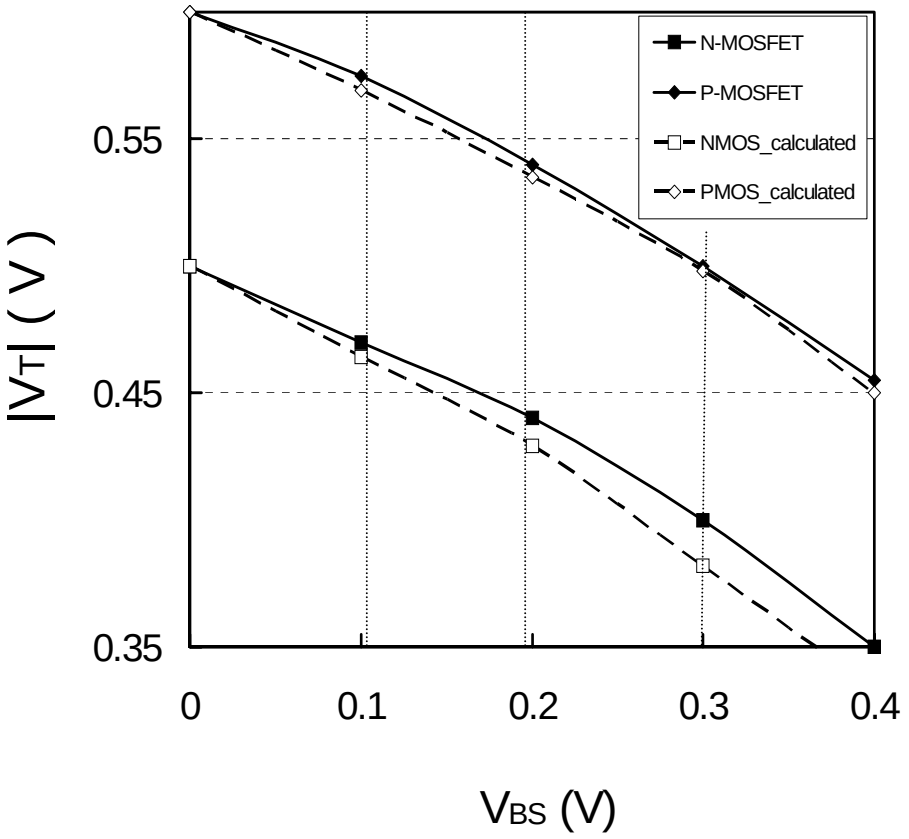


Figure 2.6: Dependence of calculated and measured magnitude of threshold voltage in n-MOSFET and p-MOSFET with magnitude of forward body-bias $|V_{BS}|$.

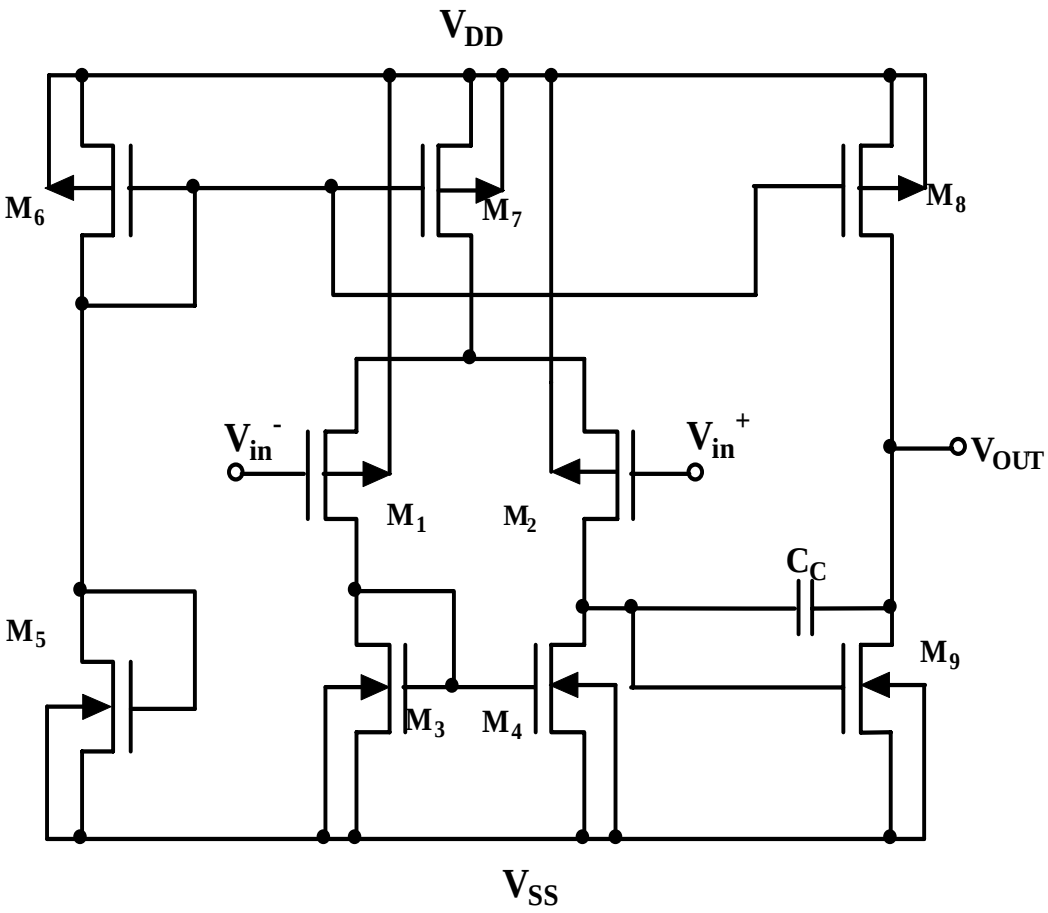


Figure 2.7: A two-stage CMOS operational amplifier.

2.3.2 Low Voltage Current Mirror Design

Current mirrors are essential parts of an operational amplifier, which are used as a load and also to provide bias currents. Figure 2.8 shows the basic CMOS current mirror circuit. For the p-MOS current mirror, we can write

$$\frac{I_{OUT}}{I_{IN}} = \frac{(W_2/L_2)}{(W_1/L_1)} \tag{2.9}$$

where W_x and L_x are the channel width and length of transistor x. The current mirror design is based on the use of non-minimum size transistors [33] to obtain a specific current ratio. In Fig. 2.8, it needs an input voltage greater than the n-MOSFET threshold voltage, V_{TN} to turn on the transistor M_1. The current mirror circuit of Fig. 2.8 is modified to a level shift current mirror as shown in Fig. 2 .9, where the bias voltage V_{DS1} can be obtained through following circuit design equations:

$$V_{DS1} = V_{GS1} - V_{SG3} \, . \tag{2.10}$$

The Eq. (2.10) describes that the bias voltage (V_{DS1}) to transistor M_1 is shifted by the gate-source voltage V_{SG3} across the transistor M_3. In the present design, M_3 is operated in the sub-threshold region ($V_{SG3} < |V_{T,P}|$).

Figure 2.10 shows a new level-shift current mirror design which combines the advantages of reduction in the threshold voltage of a forward body-biased MOSFET with the level shift circuit for low voltage operation. It also adopts output impedance enhanced architecture [34], which enhances the output impedance of the current mirror, thereby increasing the gain of the amplifier. The proposed low voltage current mirror circuit of Fig. 2.10 operates as follows. $I_{D1} = I_{D2,}$ since $V_{GS1} = V_{GS2}$ where I_{Dx} is drain current of transistor x. The transistor M_9 provides the bias current to the input transistor M_1. The

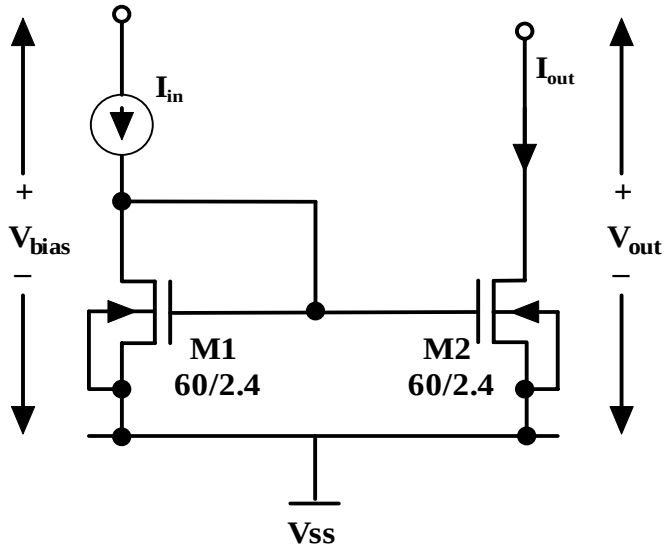


Figure 2.8: An n-MOS current mirror circuit in CMOS. The fraction indicate W/L ratio of the corresponding transistors.

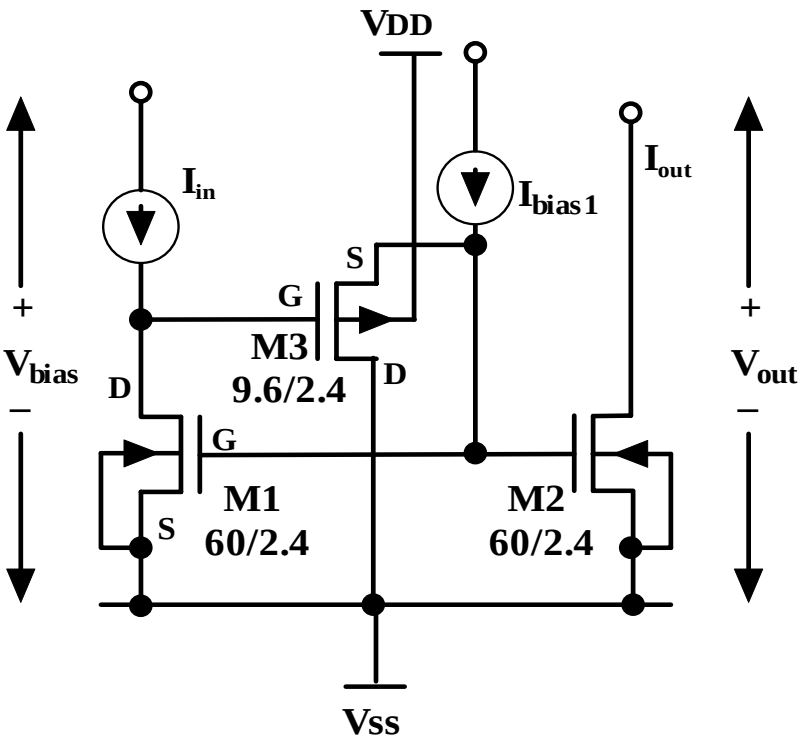


Figure 2.9: A CMOS level shift current mirror CMOS circuit. The fraction indicate W/L ratio of the corresponding transistors.

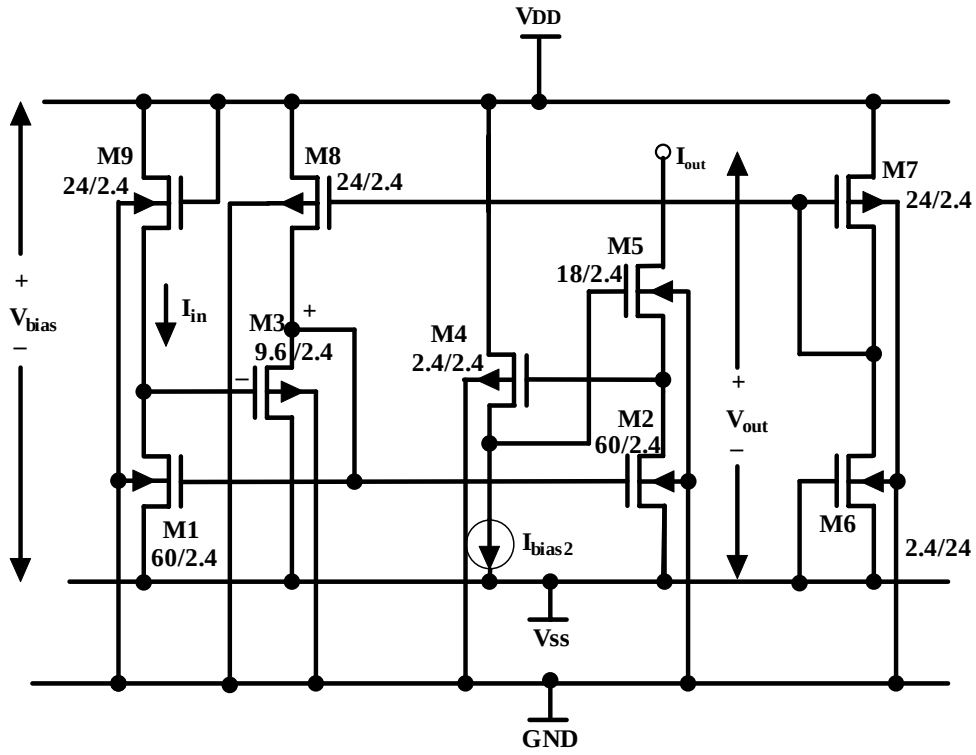


Figure 2.10: A new level shift current mirror CMOS circuit. The fraction indicate W/L ratio of the corresponding transistors.

transistor M_3 is a level shift transistor which provides a voltage drop, V_{SG3}. It sets V_{DS1} equal to $|V_{GS1} - V_{SG3}|$ as described in Eq. 2.10. Thus, V_{DS1} is reduced from V_{GS1} of the circuit of Fig. 2.8. It should be noted that $V_{SG3} < |V_{TP}|$ since M_3 is operated in sub-threshold region. The transistors, M_6, M_7 and M_8 combination provide the bias current to the level shift transistors M_3. The transistor M_5 forms as cascode configuration with the transistor M_2 and increases the output impedance of the current source. The transistor M_4 provides bias to transistor M_5.

Figure 2.11 shows the dependence of bias current I_{in} on the bias voltage, V_{bias} for current source circuits of Figures 2.8, 2.9 and 2.10, respectively. In Fig. 2.11, the solid line represents the measured characteristic and the dashed line represents the corresponding SPICE simulated characteristic. Figure 2.11 shows that a bias voltage of approximately 0.6 V is needed to get a bias current of 8 μA (c) compared to a 1.5 V for a basic current mirror circuit (a) and 1 V for a conventional level shift current mirror circuit (b). The measured and simulated I-V characteristics of the new level shift current mirror circuit of Fig. 2.10 are shown in Fig. 2.12. The output current is nearly independent of the output voltage from 0.3 to 1 V and exhibits high output impedance. The novel design of current mirror circuit of Fig. 2.10 is very suitable for the low voltage operation since it has the low output voltage and the required high output impedance.

2.3.3 Low Voltage Operational Amplifier Design

Figure 2.13 shows the circuit diagram of a two-stage CMOS amplifier for operation at ± 0.4 V. The operation of a two stage low voltage amplifier shown in Fig. 2.13 is given below. The input bias current generating circuit provides input bias current for first stage and second stage of amplifier. In the input current generating block, M_{13}

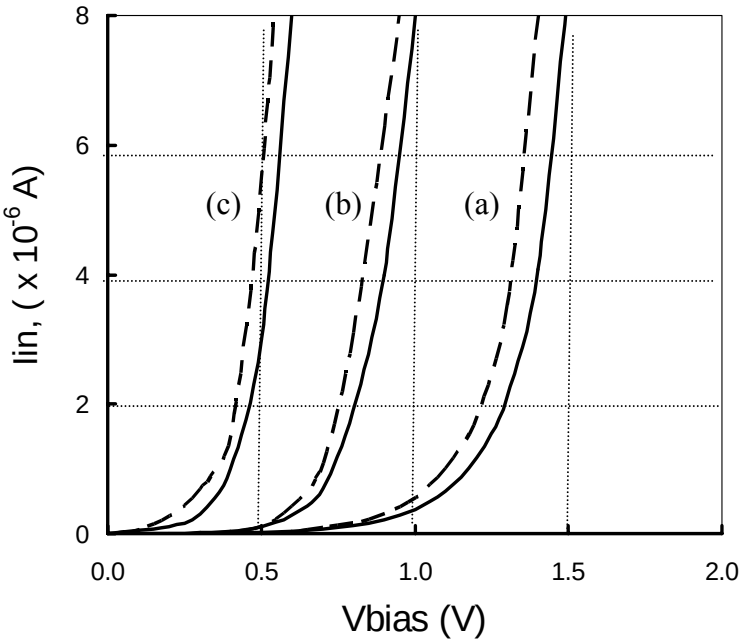


Fig. 2.11: Input bias current versus bias voltage for the current mirror circuits of Figs. 2.8, 2.9 and 2.10. (a) Basic current mirror circuit of Fig. 2.8, (b) Level shift current mirror circuit of Fig. 2.9 and (c) New level shift current mirror circuit of Fig. 2.10. Solid lines indicate measured values and dashed lines indicate simulated values.

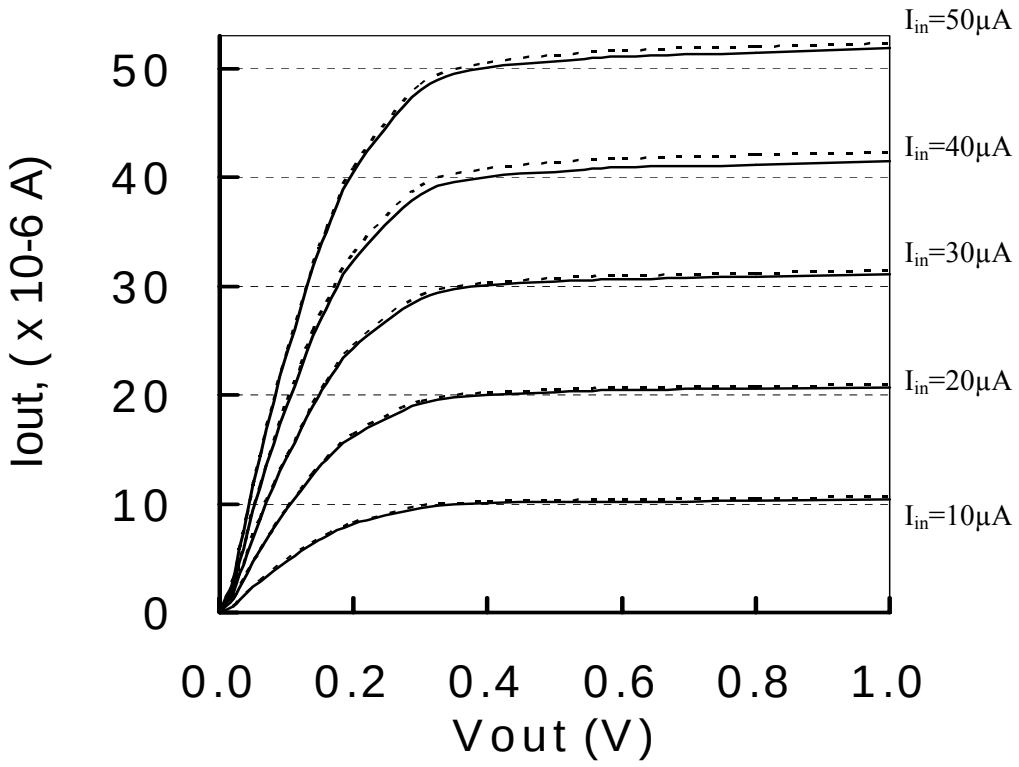


Figure 2.12: I-V characteristics of the new level shift current mirror circuit of Fig. 2.10.

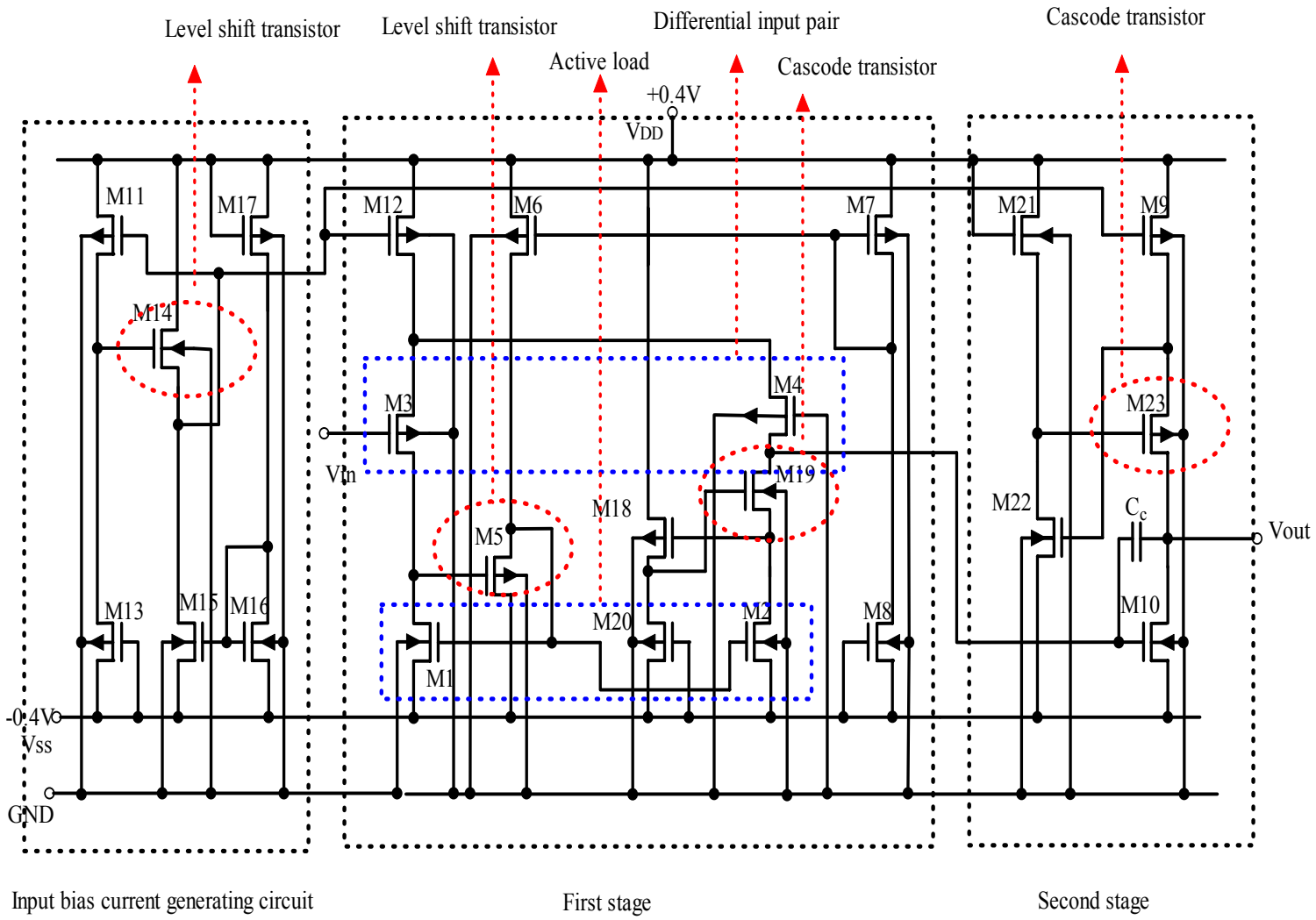


Figure 2.13: Circuit diagram of a low voltage CMOS amplifier.

provides bias current for M_{11}. M_{17} provides bias current for M_{14} through M_{15}-M_{16} current mirror.. M_{14} is a level shift transistor for M_{11}. In the first stage block, M_{12} is the corresponding transistor to mirror the input current. M_3 and M_4 are differential input pair transistors of the first stage. M_1 and M_2 are active loads for the first stage. M_5 is the level shift transistor for M_1. M_6, M_7 and M_8 combination provides bias current to M_5. M_{19} is cascode transistor to increase the output impedance. M_{20} provides bias current to M_{18} and then M_{18} biases M_{19}. In the second stage block, M_9 is the corresponding transistor to mirror the input current. M_{10} is the drive transistor of the second stage. M_{23} is the cascode transistor to increase the output impedance of the second stage. M_{21} offers bias current to M_{22} which generates voltage bias for M_{23}. C_C is for splitting poles of the two stage amplifier and improves its phase margin. The body terminals of n-MOSFETs and p-MOSFETs are tied to ground, so that both of n- and p-MOSFETs in the amplifier are forward body-biased at 0.4 V.

Table 2.1 summarizes the W/L ratios of transistors in the circuit of Fig. 2.13.

The small signal voltage gain a_v is given by

$$a_v = a_{v1} a_{v2} \tag{2.11}$$

where a_{v1} and a_{v2} are the gain of the first and second stages, respectively. Figure 2.14 shows the simplified first stage of the amplifier circuit. Figure 2.15 shows the small signal model of the first stage equivalent circuits for gain calculation. Assuming that the differential amplifier circuit in Fig. 2.14 is unloaded, we can write

$$i_{out} = g_{m4} v_{sg4} - i_1 = g_{m4} v_{sg4} - g_{m3} v_{sg3} \frac{g_{m1} r_p}{1 + g_{m1} r_p} \tag{2.12}$$

where g_{mx} is the transconductance of the transistor $M_{x.}$, r_p is $r_{ds3} // r_{ds1}$.

Table 2.1 W/L ratios of transistors in CMOS amplifier circuit of Fig. 2.13

Trans	**W/L (μm/μm)**	**Trans**	**W/L (μm/μm)**	**Trans**	**W/L (μm/μm)**
M1	60/2.4	M9	120/2.4	M17	4.8/2.4
M2	60/2.4	M10	6/2.4	M18	2.4/2.4
M3	120/2.4	M11	120/2.4	M19	18/2.4
M4	120/2.4	M12	240/2.4	M20	60/2.4
M5	9.6/2.4	M13	24/2.4	M21	2.4/2.4
M6	24/2.4	M14	4.8/2.4	M22	2.4/2.4
M7	24/2.4	M15	12/2.4	M23	24/2.4
M8	2.4/2.4	M16	12/2.4	Cc	30 pF

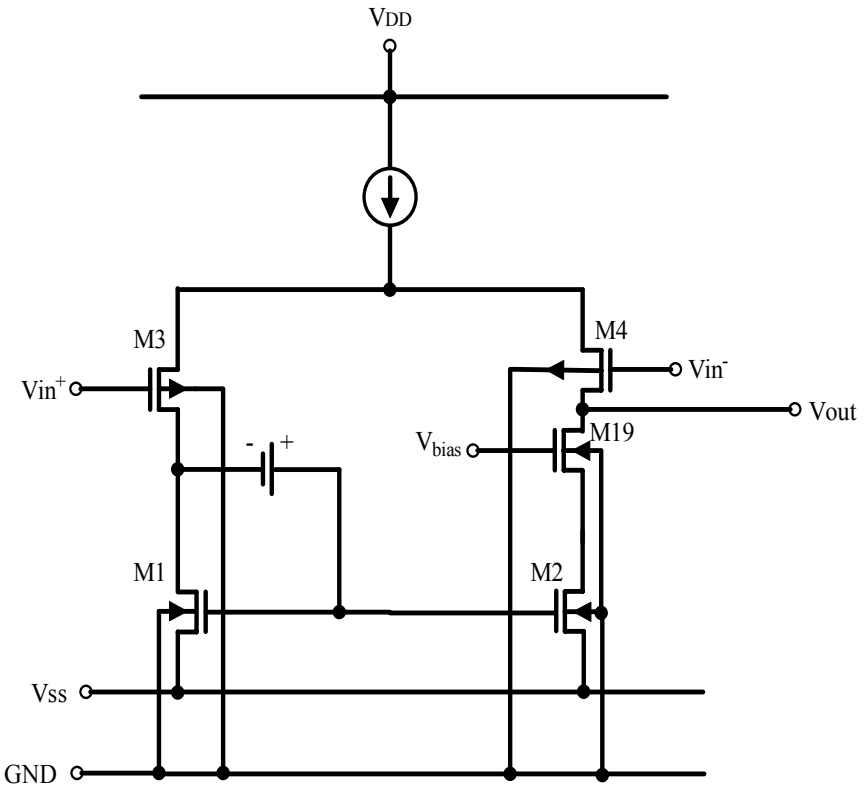


Figure 2.14: Simplified first stage circuit of amplifier circuit shown in Fig. 2.13.

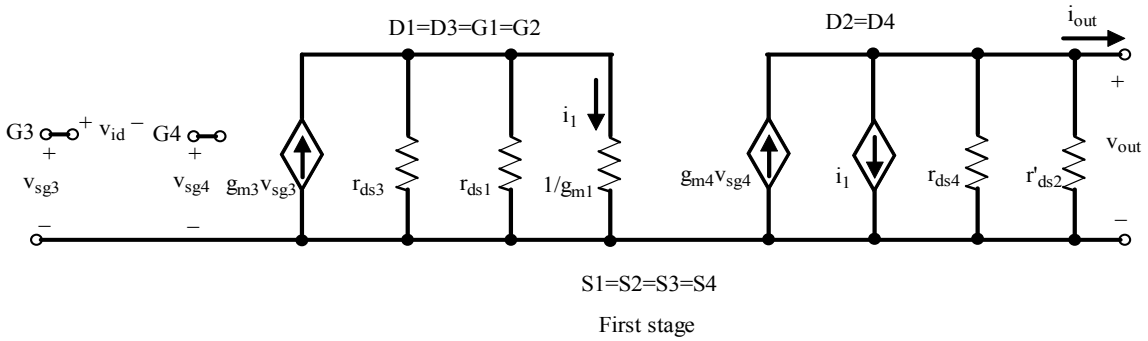


Figure 2.15: Small signal equivalent circuit for the simplified first stage circuit of Fig. 2.14. v_{id} is differential input voltage, $i_1$is current through M_1 which is mirrored to M_2. D_x is the drain of transistors and S_x is the source of transistors.

For $g_m r_p >> 1$, this simplifies to

$$i_{out} \approx g_{m4} v_{sg4} - g_{m3} v_{sg3} = g_{m3} v_{id} \tag{2.12a}$$

where $g_{m3}=g_{m4}$ and $v_{id}=v_{sg4}-v_{sg3}$. V_{out} is given by

$$v_{out} = i_{out} \times r_{out} = v_{id}\, g_{m3} (r'_{ds2} // r_{ds4}) . \tag{2.13}$$

Here, r'_{ds2} is the parallel combination of r'_{ds2} and r_{ds4}. r'_{ds2} is the cascode stage output resistance and r_{dsn} is the output resistance of the M_n transistor. r'_{ds2} is expressed by

$$r'_{ds2} = g_{m19} r_{ds2} r_{ds19} . \tag{2.14}$$

Thus, the gain of first stage amplifier is given by

$$a_{v1} = g_{m3} \{ r_{ds4} // (g_{m19} r_{ds2} r_{ds19}) \} . \tag{2.15}$$

Figure 2.16 shows the simplified circuit of the second stage of the amplifier. The corresponding small signal equivalent circuit is shown in Fig. 2.17. From Fig. 2.17, we can write

$$g_{m10} v_{gs10} + \frac{v_{out}}{r_{ds10}} + \frac{v_{out}}{r'_{ds9}} = 0 \tag{2.16}$$

where r'_{ds9} is the equivalent cascode resistance and is given by

$$r'_{ds9} = g_{m23} r_{ds23} r_{ds9} . \tag{2.17}$$

The second stage gain is calculated from Eq. (2.16) as follows:

$$a_{v2} = \frac{v_{out}}{v_{gs10}} = -g_{m10} (r_{ds10} // r'_{ds9}) . \tag{2.18}$$

Substituting Eq. (2.17) in Eq. (2.18), we obtain

$$a_{v2} = -g_{m10} \{ r_{ds10} // (g_{m23} r_{ds9} r_{ds23}) \} . \tag{2.19}$$

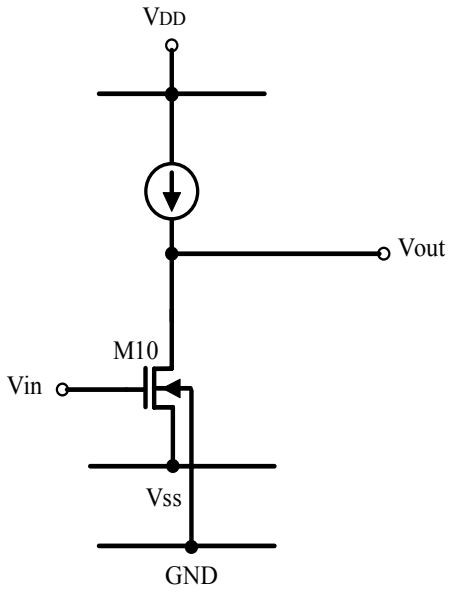


Figure 2.16: Simplified circuit for the second stage of the amplifier circuit shown in Fig. 2.13.

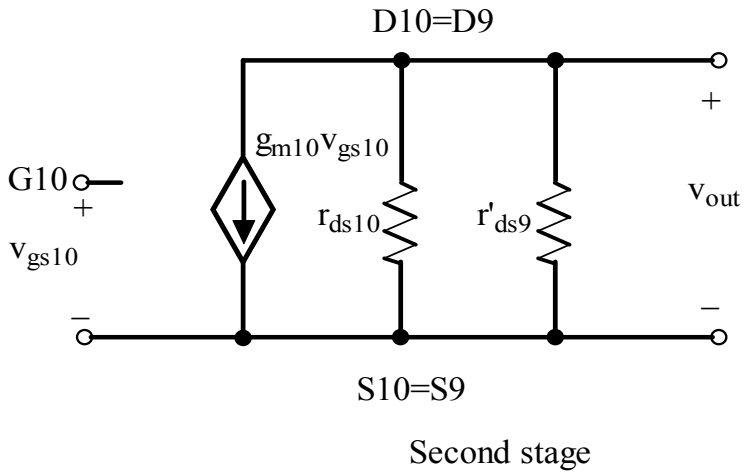


Figure 2.17: Small signal equivalent circuit of the second stage of the amplifier shown in Fig. 2.16. D_x is the drain of transistors and S_x is the source of transistors.

2.3.4 Simulated and Experimental Results

Figure 2.18 shows the chip layout of the CMOS amplifier circuit of Fig. 2.13. Figure 2.19 shows the microphotograph of the fabricated CMOS amplifier circuit. Figure 2.20 shows the measured input-output amplifier voltage response. Figure 2.21 shows the frequency response characteristics. Table 2.2 summarizes the measured parameters obtained from Figs. 2.20 and 2.21. The corresponding SPICE simulated values are also included for comparison. Table 2.2 shows that the designed and simulated parameters are in close agreement with the corresponding measured values. Appendix C describes several measurement techniques [35] used in extracting amplifier parameters summarized in Table 2.2. In Table 2.3, measured parameters of the amplifier are compared with the corresponding parameters reported in recent publications [13, 14]. The open loop gain for the present amplifier design is nearly 10 dB higher in comparison to gain reported in [13, 14]. The 3 dB bandwidth is also increased. The other measured parameters are in close agreement.

2.4 Summary

An ultra-low power amplifier has been designed for operation at ± 0.4 V in 1.5 μm n-well CMOS technology using the forward body-bias technique. The forward body-bias is limited to 0.4 V to avoid CMOS latchup. The measured gain is nearly 58 dB with a 3 dB 30 kHz bandwidth. The power consumption of 80 μW is extremely low. Compared with the recently reported low voltage amplifier designs [13, 14], open loop gain is increased by 10 dB. The present low power CMOS amplifier can be used in portable devices, biomedical instrumentation and microsystems [17, 22].

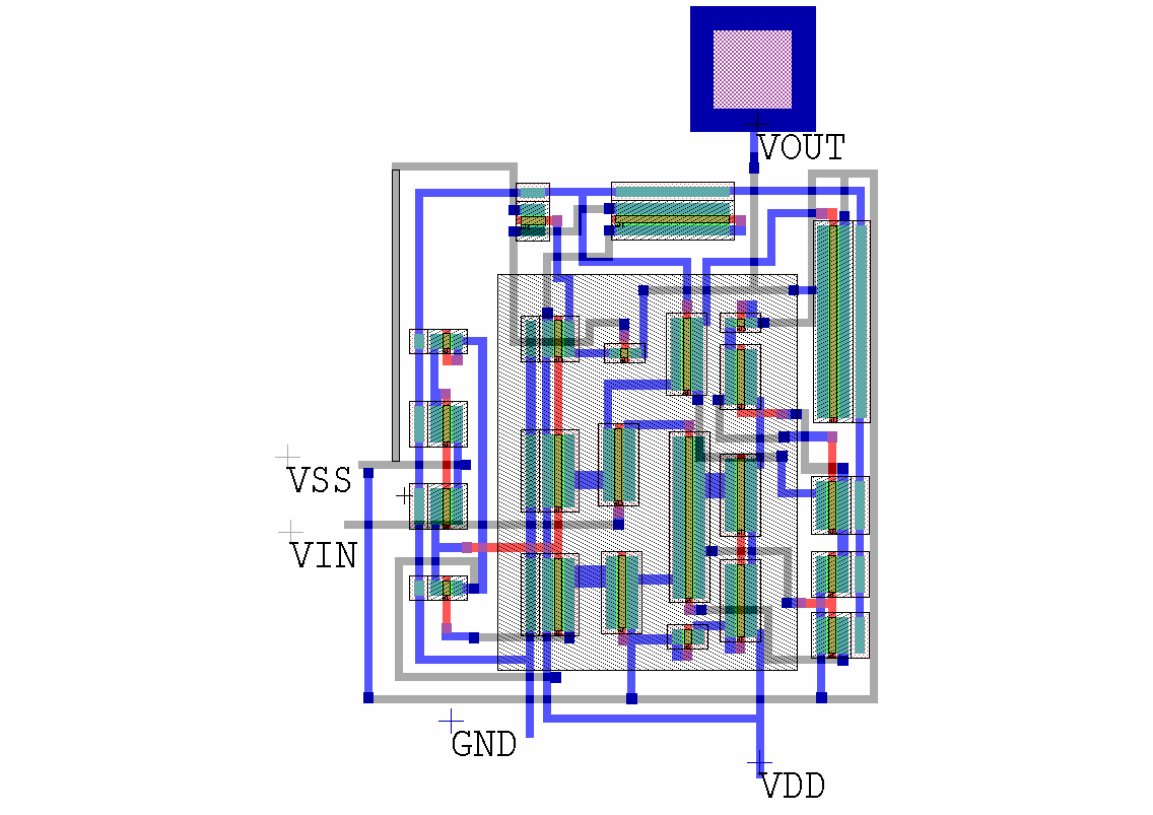


Figure 2.18: Chip layout of the CMOS amplifier circuit of Fig. 2.13.

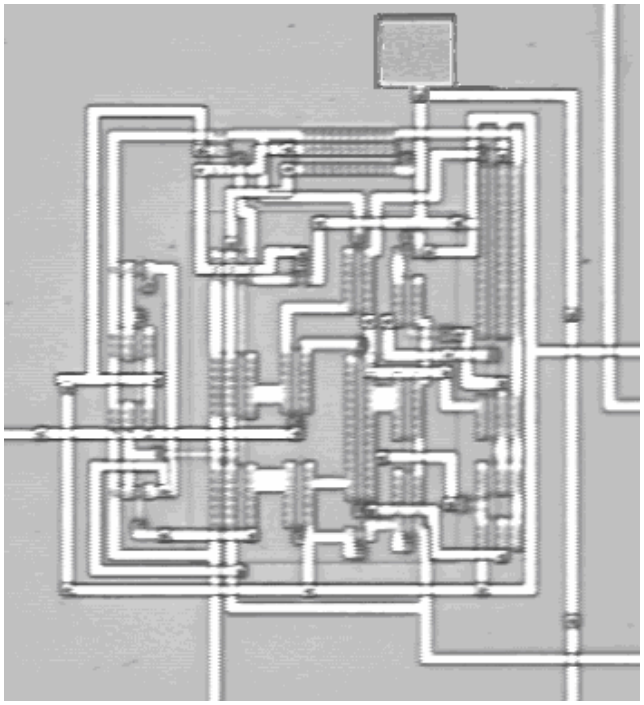


Figure 2.19: Microphotograph of the fabricated IC chip containing circuit of Fig. 2.13.

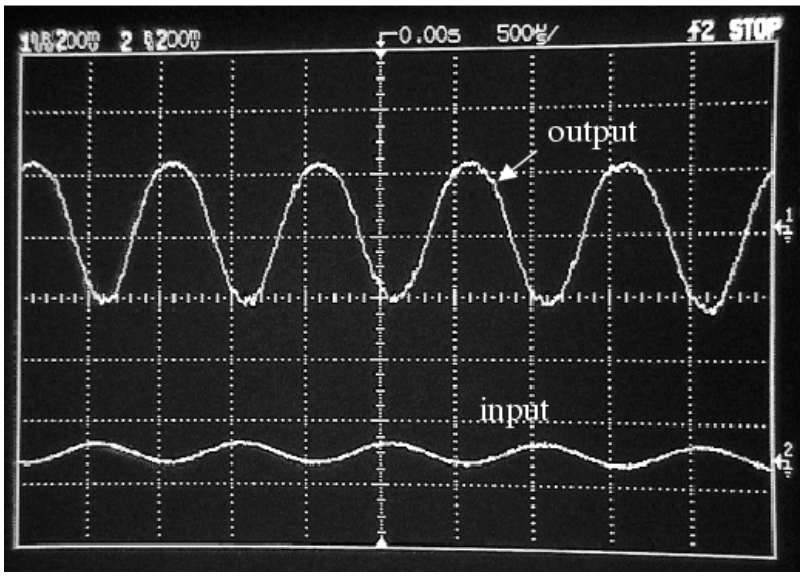


Figure 2.20: Measured input-output waveforms at 1 kHz of the CMOS amplifier circuit of Fig. 2.13. X-axis: 50 μS/div, Y-axis: 200 mV/div. Input waveform shown is enlarged 200 times.

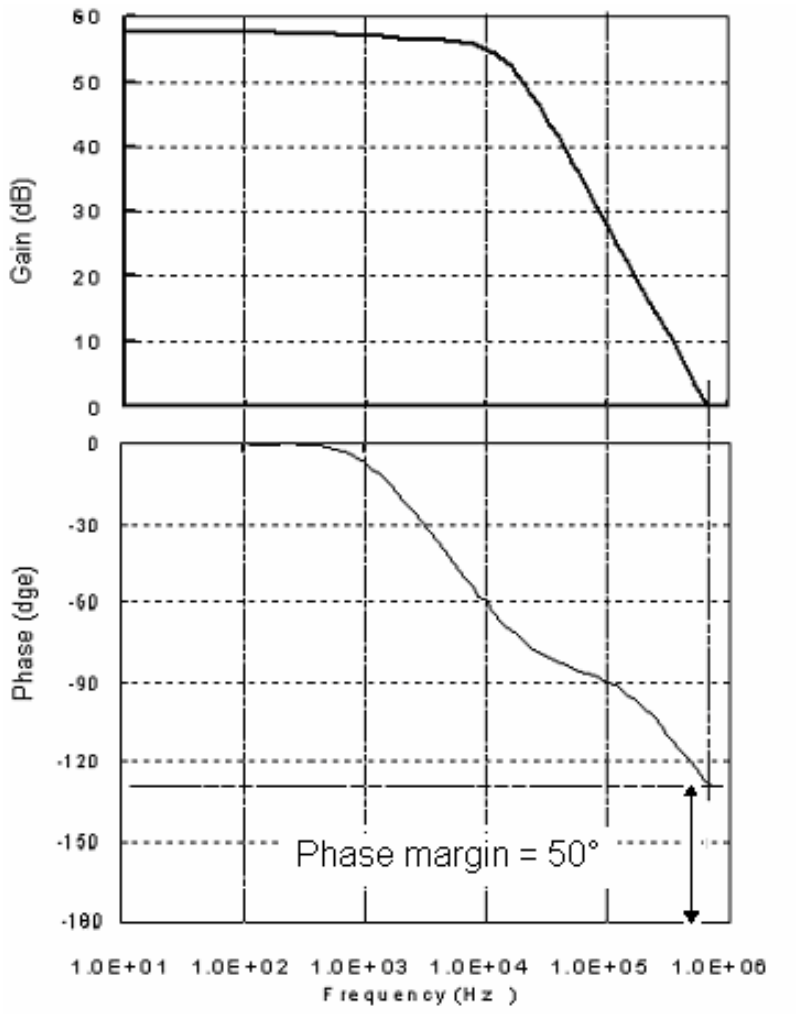


Figure 2.21: Measured frequency response characteristics of the low-power CMOS amplifier circuit of Fig. 2.13. Phase margin is 50^{o}.

Table 2.2 Measured and simulated parameters of the CMOS amplifier circuit of Fig. 2.13.

Parameters	**Simulated Results (SPICE)**	**Measured Results**
Supply voltage	± 0.4 V	± 0.4 V
Open-loop gain	70 dB	58 dB
3-dB bandwidth	30 kHz	30 kHz
Phase margin	45^{o}	50^{o}
Input common-mode range (ICMR)	- 0.4 V to 0.1 V	-0.4 V to 0 V
Output voltage swing	- 0.35 V to 0.35 V	-0.35V to 0.3 V
Power dissipation	60 µW	80 µW
Unity gain bandwidth	1 MHz	0.7 MHz
Slew rate (SR^{+}) Slew rate (SR^{-})	0.2 V/µS 0.5 V/µS	0.1 V/µS 0.3 V/µS
V_{DD} Power supply rejection ratio (PSSR)	70 dB at 10 kHz	60 dB at 10 kHz
V_{SS} Power supply rejection ratio (PSSR)	60 dB at 10 kHz	40 dB at 10 kHz
Output offset voltage (V_{os})	—	1 mV
Common-mode rejection ratio (CMRR)	54 dB at 10 kHz	50 dB at 10 kHz

Note: − represents data which are not available.

Table 2.3 A comparative study of the present amplifier characteristics with the corresponding parameters reported in recent publications.

Parameters	**Measured [13]**	**Measured [14]**	**Measured [current design]**
Supply voltage	± 0.5 V	0.8 V	± 0.4 V
Open-loop gain	49 dB	46 dB	58 dB
3-dB bandwidth	10 kHz	—	30 kHz
Phase margin	57^{o}	54^{o}	50^{o}
Input common-mode range (ICMR)	- 0.49 V - 0.5 V	0 V - 0.4 V	-0.4 V - 0 V
Output voltage swing	- 0.35 V - 0.35 V	0.15 V - 0.65 V	-0.35 V - 0.3 V
Power dissipation	287 µW	—	80 µW
Unity gain bandwidth	1.3 MHz	0.8 MHz	0.7 MHz
Slew rate (SR^{+}) Slew rate (SR^{-})	0.7 V/ µS 1.6 V/ µS	0.4 V/ µS —	0.1 V/ µS 0.3 V/ µS
V_{DD} Power supply rejection ratio (PSSR)	61 dB at 10 kHz	—	60 dB at 10 kHz
V_{SS} Power supply rejection ratio (PSSR)	45 dB at 10 kHz	—	40 dB at 10 kHz
Output offset voltage (V_{os})	1.2 mV	—	1 mV
Common-mode rejection ratio (CMRR)	—	—	50 dB at 10 kHz

Note: − represents data which are not available.

CHAPTER 3

NOISE ANALYSIS OF A FORWARD BODY-BIAS CMOS AMPLIFIER [*]

Noise is a major problem in the design of an amplifier for low-voltage application. Here the noise can become comparable to the amplitude of the signal. This chapter focuses on the noise analysis of a forward body-bias MOSFET. Noise model of a MOSFET, which includes effect of the forward-body bias, is proposed. Noise analysis of a forward body-bias CMOS amplifier designed in Chapter 2 is described. Analytical and simulation results from the SPICE are presented and discussed.

3.1 Noise in the MOSFET

Electrical noises limit the low voltage processing of input signals. If the noise level approaches the input signal, it will deteriorate the signal quality. The following three types of noises: flicker noise, thermal noise and shot noise are associated with a MOSFET. The flicker noise, which is also known as 1/f noise, relates to variations in processing parameters and dominates at lower frequencies. It is expressed as follows [18]

$$\frac{\overline{i_{1/f}^{\,2}}}{\Delta f} = \alpha \frac{I_D}{f} \tag{3.1}$$

where $\overline{i_{1/f}^{\,2}}/\Delta f$ is the flicker noise current spectral density. α is a constant for a particular device. I_D is direct current and f is the frequency. Equation (3.1) describes that the flicker noise is proportional to the dc current flow and has a $1/f$ frequency dependence.

[*] Part of this work is reported in following publications:

1. C. Zhang, A. Srivastava and P. K. Ajmera, "Noise analysis in a 0.8 V forward body-bias CMOS op-amp design," Fluctuation and Noise Letters (FNL)-Special issue on Noise in Device and Circuits, vol. 4, No. 2, pp. L403-L412, 2004.
2. C. Zhang, A. Srivastava and P. K. Ajmera, "Noise analysis of an ultra-low power CMOS operational Amplifier Circuit," *Proc. of SPIE*, Vol. 5113, pp. 294-300, 2003.

The shot noise in a diode is described by

$$\frac{\overline{i_s^2}}{\Delta f} = 2qI_{DC} \tag{3.2}$$

where $\overline{i_s^2}/\Delta f$ is the shot noise current spectral density and is proportional to current, I_{DC} in a forward-biased p-n junction. The shot noise is caused by the carriers which cross through a potential barrier. The possibility of each carrier crossing the potential barrier is random in nature. Thus dc current across the p-n junction is composed of a large number of random current pulses.

The thermal noise in a MOSFET is described by

$$\frac{\overline{v_{thermal}^2}}{\Delta f} = \frac{8}{3}kT\frac{1}{g_m} \tag{3.3}$$

where $\overline{v_{thermal}^2}/\Delta f$ is the thermal noise voltage spectral density related to V_{gs} for a MOSFET in saturation, k is the Boltzman's constant, T is absolute temperature and g_m is the device transconductance. Thermal noise is inversely proportional to the transconductance, g_m.

Recently, 1/f noise has been reported in forward body-biased MOSFETs [19]. However, there are no published papers covering a more complete analysis of the noise associated with a forward body-biased MOSFET. In this chapter, noise model is developed for a forward body-biased MOSFET and used in the noise analysis of a 0.8 V forward body-biased CMOS operational amplifier design presented in Chapter 2.

3.2 Noise in a Forward Body-Biased n-MOSFET

The shot noise in a MOSFET under the reverse body-biased condition can be neglected since number of carriers crossing the source-substrate reverse biased p-n junction is very small. But the shot noise will increase significantly under a forward

body-biased condition since the carriers across the junction increase exponentially. Thus, the forward body-bias should be limited to a certain level to avoid introducing significant noise especially when it becomes comparable to the input signal. The shot noise current spectral density can be converted to an equivalent noise voltage spectral density by multiplying Eq. (3.2) by the p-n junction impedance, $1/\ j\omega c_{sb}$. The angular frequency is ω and the source-substrate junction capacitance is c_{sb}. Figure 3.1 shows the SPICE simulated variation of the shot noise and the thermal noise in a forward body-biased n-MOSFET obtained at a 10 kHz signal. From Fig. 3.1, it can be seen that the thermal noise of a MOSFET decreases with increasing the forward bias between the source-substrate junction. The forward-biased substrate reduces the threshold voltage, which increases the transconductance, g_m and hence reduces the thermal noise. However, the shot noise in an n-MOSFET increases with increasing forward body-bias as shown by the dotted line in Fig. 3.1 and is due to increase in conduction of the source-substrate p-n junction diode. It is concluded from Fig. 3.1 that the shot noise is negligible when forward bias is less than 0.3 V but increases exponentially with increasing forward body-bias. It is comparable to the magnitude of the thermal noise under a forward body-bias of 0.4 V. Total noise of the device still increases regardless of decreasing thermal noise beyond forward body-bias 0.4 V. Thus, from noise analysis point of view also, a forward body-bias greater than 0.4 V is not recommended. Since the total noise introduced by a limited forward body-bias is not significant, forward body-biased technique to design low-power op-amp is feasible.

Figure 3.2 shows the small signal noise model of a forward body-biased MOSFET. In Fig. 3.2, $\overline{i_g^{\,2}}$ is gate leakage current noise generator, $\overline{i_d^{\,2}}$ is the drain current noise generator, $\overline{i_s^{\,2}}$ is the substrate leakage current noise generator, $g_m v_{gs}$ is the current

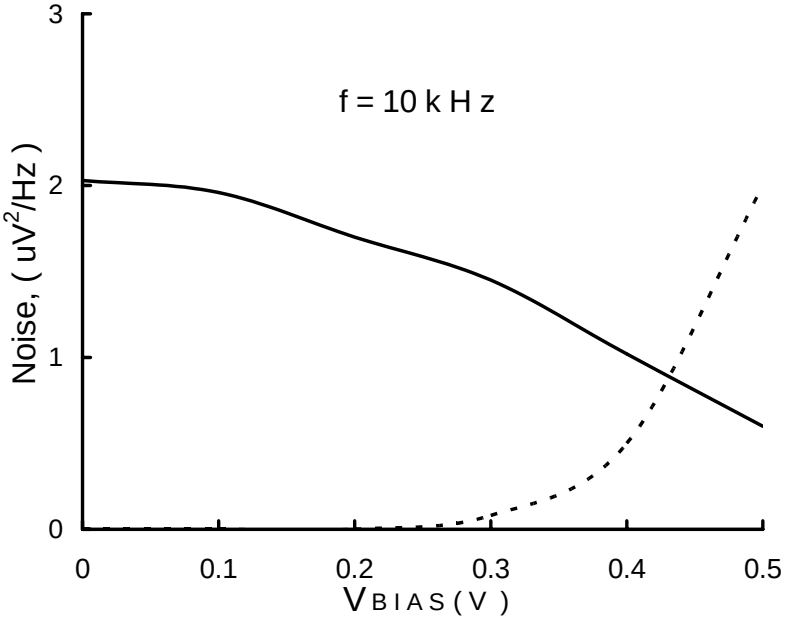


Figure 3.1: Equivalent noise voltage spectral density variation with forward body-bias corresponding to shot noise (dotted line) and thermal noise (solid line) in an n-MOSFET.

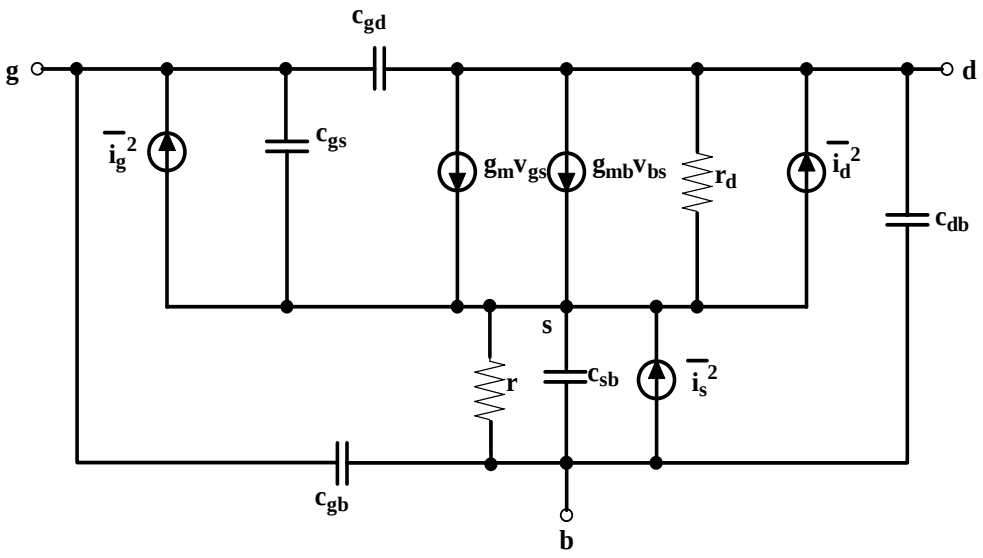


Figure 3.2: Small signal noise model of a forward body-biased n-MOSFET. Source, drain, gate and substrate are denoted by s, d, g and b, respectively.

source due to gate source voltage, $g_{mb}v_{bs}$ is current source due to body source voltage, r_d is the small signal output resistance, c_{gb}, c_{gd}, c_{gs}, c_{sb} and c_{db} are capacitances associated with a MOSFET.

In the noise analysis for a MOSFET [18], usually substrate leakage current noise generator $\overline{i_s^2}$ is not included since its value is small under the reverse body-biased condition. However, $\overline{i_s^2}$ should be included in the noise model for the forward body-biased MOSFET as the leakage current now increases exponentially with the forward body-bias. The equivalent input referred current noise generator can be calculated by equating all current sources to output currents [18]. We obtain

$$\frac{g_m}{j\omega c_{gs}} i_i = i_g \frac{g_m}{j\omega c_{gs}} + i_d + i_s \frac{g_{mb}}{j\omega c_{sb}} \tag{3.4}$$

where i_i is the equivalent rms value of the input noise current. The currents i_g, i_d, i_s are the rms values of the current noise sources corresponding to the gate leakage current, drain-source current, and the substrate leakage current, respectively. Equation (3.4) does not include the effects of c_{gb}, c_{db} and c_{gd}. In Eq.(3.4), g_{mb} is transconductance of the source-substrate n^+-p junction. Since i_g, i_d and i_s are independent, we can disregard phase relationships and write

$$\overline{i_i^2} = \overline{i_g^2} + \overline{i_d^2} \frac{\omega^2 c_{gs}^2}{g_m^2} + \overline{i_s^2} \frac{c_{gs}^2}{c_{sb}^2} \frac{g_{mb}^2}{g_m^2} \tag{3.5}$$

where $\frac{\overline{i_d^2}}{\Delta f} \approx \frac{8}{3} kTg_m$, $\frac{\overline{i_g^2}}{\Delta f} = 2qI_G$ and $\frac{\overline{i_s^2}}{\Delta f} = 2qI_S$. I_G is the gate current and I_S the body leakage current. It should be noted that noise current spectral density $\overline{i_d^2}/\Delta f$ is the sum

of contributions from both the thermal noise and flicker noise and is given by $\overline{i_d^{\,2}}/\Delta f = (8/3)kTg_m + K\, I_D^a / f$ where K is constant and a is constant between 0.5 and 2.

Deen and Marinov [19] have shown quadratic dependence of flicker noise on the drain current. The flicker noise normally dominates at frequency below 10-100 kHz. In a low voltage amplifier design presented, very low drain current (20 % drain current compared to a 5 V regular CMOS amplifier) flows in a transistor. The low drain current reduces the flicker noise. The forward substrate bias also lowers the flicker noise by 9 dB/V at a fixed I_D when the MOSFET is in strong inversion [19]. Flicker noise corner frequency where flicker noise is equal to white noise is also pushed back to the lower frequency of 100 Hz to 1 kHz, which is lower than 10 kHz frequency at which shot noise and thermal noise are calculated in Fig. 3.1.

In Equation (3.5), the thermal noise density part is given by

$$\frac{\overline{i_{i\,thermal}^{\,2}}}{\Delta f} = \frac{\overline{i_d^{\,2}}}{\Delta f}\frac{\omega^2 c_{gs}^{\,2}}{g_m^{\,2}} = \frac{8}{3}kT\frac{\omega^2 c_{gs}^{\,2}}{g_m}. \tag{3.6}$$

The shot noise density part is obtained by substituting Eq. (3.2) in Eq. (3.5) and is given by

$$\frac{\overline{i_{i\,shot}^{\,2}}}{\Delta f} = 2qI_G + \frac{\overline{i_s^{\,2}}}{\Delta f}\frac{c_{gs}^{\,2}}{c_{sb}^{\,2}}\frac{g_{mb}^{\,2}}{g_m^{\,2}}. \tag{3.7}$$

Neglecting gate current, we obtain

$$\frac{\overline{i_{i\,shot}^{\,2}}}{\Delta f} \approx 2qI_{S0}(e^{-V_{SB}q/kT} - 1)\frac{c_{gs}^{\,2}}{\dfrac{c_{sbo}^{\,2}}{(1+V_{SB}/\psi_o)}}\frac{\gamma^2}{4(2\phi_f + V_{SB})} \tag{3.7a}$$

where $C_{sb} = \dfrac{C_{sbo}}{(1+V_{SB}/\psi_o)^{1/2}}$ and $\dfrac{g_{mb}^{\,2}}{g_m^{\,2}} = \dfrac{\gamma^2}{4(2\phi_f + V_{SB})}$.

In Eq. (3.7a), V_{SB} is the source-body voltage and is positive when it is reverse biased, I_{so} is a reverse saturation current of the source-body junction diode, C_{sbo} is the source-body junction parasitic capacitor at zero bias, ψ_o is build-in potential, $\phi_f = \{(kT/q) \ln (N_A/n_i)\}$ is the surface potential for the substrate and γ is the body coefficient parameter for the MOSFET. Since the gate current I_G is usually negligibly small, the first term in Eq. (3.7a) is neglected. Substrate leakage current noise generator, $\overline{i_s^2}$ in Eq. (3.7a) is put in the form of a gate-referred noise generator. It is determined by the current across the source-substrate junction, which is biased by V_{SB} and is independent of V_{GS}-V_T. In the present design, a forward body-bias of 0.4 V is taken which is not only to avoid CMOS latchup [15] but also to keep the total noise low.

3.3 Noise Analysis of a Forward Body-Bias CMOS Amplifier Circuit

Figure 3.3 is the circuit diagram of a two-stage CMOS op-amp and is same as Figure 2.13 and repeated here for noise modeling. SPICE simulations for the designed amplifier give a gain of 70 dB and 3-dB bandwidth of 30 kHz. The input signal is a 10 kHz sine wave of 50 μV peak-to-peak amplitude. The output waveform is a sine wave of peak-to-peak amplitude 350 mV. The power dissipation is 80 μW. These post-layout simulation values have been obtained from SPICE utilizing level 3 MOS model parameters.

The noise in an op-amp can be calculated using the noise model [18] as shown in Fig. 3.4 where $\overline{v_{eq_1}^2}, \overline{v_{eq_2}^2}, \overline{v_{eq_3}^2}$ and $\overline{v_{eq_4}^2}$ are equivalent input voltage noise generators for transistors M_1 to M_4. M_3 and M_4 are differential input devices. Differential input signal is applied to M_3 and M_4. Since the input differential stage of an amplifier has large current

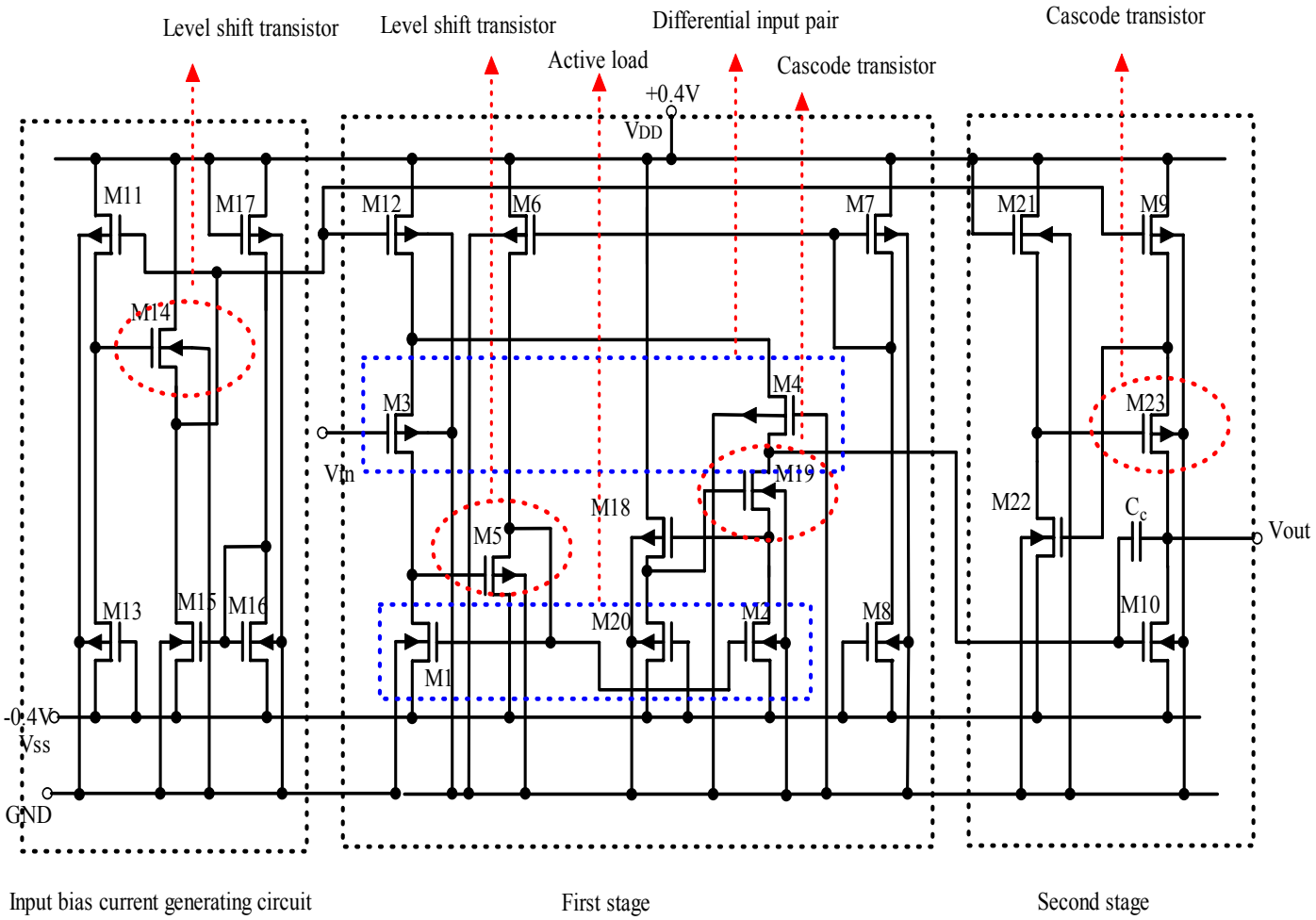


Figure 3.3: Circuit diagram of a low voltage CMOS amplifier. Figure 3.3 is same as Fig. 2.13.

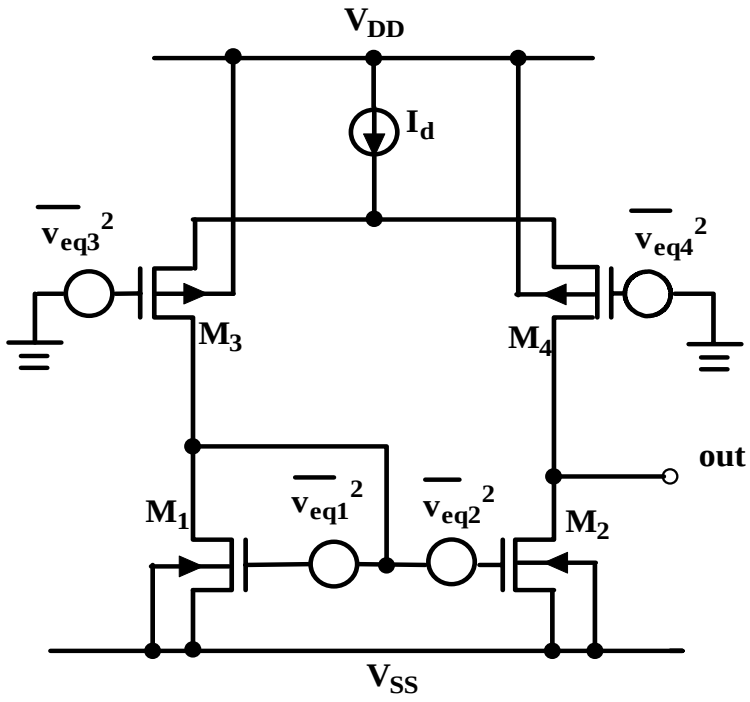


Figure 3.4: Noise model of a CMOS differential pair amplifier.

and voltage gains, the noise associated with the following stages are insignificant in comparison to input referred noise of the differential stage [18].

Equating them to total equivalent input voltage noise generator, and assuming M_1, M_2 are identical and M_3 and M_4 are identical, the total equivalent input voltage noise generator, $\overline{v_{eq\_total}^{\,2}}$ can be written as

$$\overline{v_{eq\_total}^{\,2}} = \overline{v_{eq3}^{\,2}} + \overline{v_{eq4}^{\,2}} + \left(\frac{g_{m1}}{g_{m3}}\right)^2 (\overline{v_{eq1}^{\,2}} + \overline{v_{eq2}^{\,2}}) . \tag{3.8}$$

Major contribution to noise in an op-amp comes from the differential pair input stage. Converting current noise generators in Eqs. (3.6) and (3.7) into voltage noise generators, we obtain

$$\frac{\overline{v_{i\ thermal}^{\,2}}}{\Delta f} = \frac{\overline{i_d^{\,2}}}{\Delta f}\frac{1}{g_m^{\,2}} = \frac{8}{3}kT\frac{1}{g_m} \text{ and} \tag{3.9}$$

$$\frac{\overline{v_{i\ shot}^{\,2}}}{\Delta f} = \frac{\overline{i_s^{\,2}}}{\Delta f}\left|z^2\right|\frac{g_{mb}^{\,2}}{g_m^{\,2}} = 2qI_{S0}(e^{-V_{SB}q/kT} - 1)(r_{equ,s} \,//\, \frac{1}{\omega c_{sb}})^2 \frac{\gamma^2}{4(2\phi_f + V_{SB})} \tag{3.10}$$

where z is the equivalent load impedance and $r_{equ,s}$ is the equivalent output resistance of the current source. It is because sources of differential inputs of p-MOSFETs in Fig. 3.4 are connected with a current source, I_d in the op-amp design. In small-signal equivalent circuit of Fig. 3.4, $r_{equ,s}$ will appear in parallel with c_{sb}. For an ideal current source, $r_{equ,s}$ is infinite. Neglecting flicker noise and substituting Eq. (3.9) and (3.10) in Eq. (3.8), we obtain

$$\frac{\overline{v_{eq\_total}}^2}{\Delta f} = \frac{16}{3} kT \frac{1}{g_{m3}}$$
$$+ 4qI_{S0}(e^{-V_{SB}q/kT} - 1)(r_{equ,s} // \frac{1}{\omega c_{sb}})^2 \frac{\gamma^2}{4(2\phi_f + V_{SB})}$$
$$+ \left(\frac{g_{m1}}{g_{m3}}\right)^2 (\frac{16}{3} kT \frac{1}{g_{m1}}$$
$$+ 4qI_{S0}(e^{-V_{SB}q/kT} - 1)(r_{equ,s} // \frac{1}{\omega c_{sb}})^2 \frac{\gamma^2}{4(2\phi_f + V_{SB})}) \quad . \qquad (3.11)$$

Equation (3.11) gives the value of the input referred noise. It is transferred to the output as an output noise and plotted in Fig. 3.5 as a dotted line. Figure 3.5 also shows the SPICE simulated total output noise of the ultra low-power op-amp by the solid line. In Figure 3.5, it is seen that the calculated output noise of ultra low-power op-amp is 413 x 10^{-12} V^2/Hz over the op-amp 3-dB bandwidth, which is above the simulated results of 360 x 10^{-12} V^2/Hz. The simulated equivalent input noise spectral density is 227 nV/√Hz, which is obtained by dividing the output noise by the amplifier gain and taking the square root of the value. The simulated input noise spectral density is in close agreement with the corresponding 300 nV/√Hz input noise spectral density of CMOS operational amplifier of TI 1.8 V OPA349. In Fig. 3.5, the marginal difference between simulated results and calculated values from model Equation (3.11) is due to increase in shot noise in a forward body-biased MOSFET as shown in Fig. 3.4.

3.4 Summary

Noise introduced by the forward body-bias in an n-MOSFET is analyzed. The simulations show that the thermal noise decreases and shot noise increases with increasing forward bias between the source and substrate junction in a MOSFET. The shot noise increases exponentially with increasing forward body-bias. The shot noise

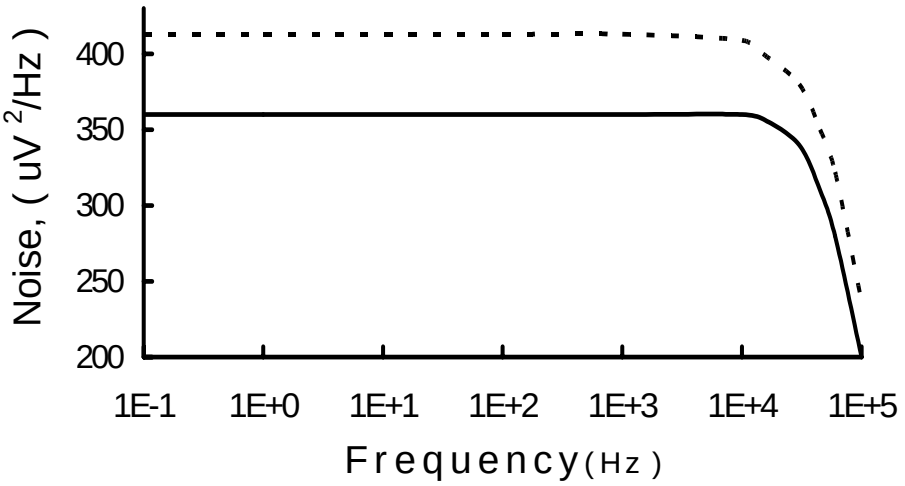


Figure 3.5: SPICE simulated (solid) and calculated (dotted) total output noise of an ultra low-power CMOS op-amp. Flicker noise is neglected.

becomes significant over the thermal noise for the forward body-bias above 0.4 V at 10 kHz. The flicker noise (1/f noise) is not considered because the low drain current and forward body-bias conditions in a MOSFET suppress it. An ultra low-power (±0.4 V) amplifier is designed using the forward body-biased technique. An amplifier gain of nearly 70 dB is achieved with a 3-dB 30 kHz bandwidth. The total power consumption is only 80 μW.

The output noise of ultra low-power amplifier is 360 x 10^{-12} V^2/Hz. It is shown that the 0.4 V forward body-bias technique combined with low voltage operation does not introduce significant noise in CMOS ultra-low power op-amp and does not trigger the latchup action. The simulated input noise spectral density of the forward body-biased CMOS operational amplifier is in close agreement with the corresponding value of TI OPA349 CMOS operational amplifier.

CHAPTER 4*

DYNAMIC THRESHOLD MOSFET TECHNIQUE

In Chapter 2, the forward body-biased MOSFET has been used for designing a low power CMOS amplifier. In the past, the method has been used for digital applications [15]. However, the method has a drawback. When the transistor is turned-off, the leakage current increases due to electrically reduced threshold voltage. The leakage current increases rapidly with the reduction of threshold voltage. Figure 4.1 shows the leakage current of a forward body-biased CMOS inverter. With increasing forward body-bias, the leakage current increases significantly. This leakage current can be reduced using a dynamic body bias technique [12]. Figure 4.2 shows a dynamic threshold MOS (DTMOS) inverter in CMOS where the gate terminals of n- and p-MOSFETs are tied to their body-terminals, respectively. In this chapter, the DTMOS technique is proposed to overcome the drawback which is inherent in the forward biased MOSFET. It operates in two modes. In the "on" mode of the transistor, the source and substrate of MOSFEET is forward biased. The threshold voltage is reduced to help in turning-on of the transistor. In the "off" mode, the transistor is switched to a zero biased source-substrate mode ($V_{SB} = 0$) in order to increase the threshold voltage. Thus, it helps to reduce the standby leakage current and turns-off the transistor completely. This chapter is focused on using the DTMOS method with the forward source-body biased MOSFETs for the low-voltage operation of CMOS VLSI circuits. CMOS analog multiplexer and Schmitt trigger circuits have been designed for low-voltage and low power applications.

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* Part of this work is reported in following publications:
1. C. Zhang, A. Srivastava and P. K. Ajmera, "0.8-V ultra low-power CMOS analog multiplexer for remote biological and chemical signal processing," *Proc. of SPIE*, Vol 5389, pp.13-19, 2004.
2. C. Zhang, A. Srivastava and P. K. Ajmera, "Low voltage CMOS Schmitt trigger circuits," *Electronics letters*, Vol. 39, No. 24, pp. 1696-1698, 27th Nov. 2003.

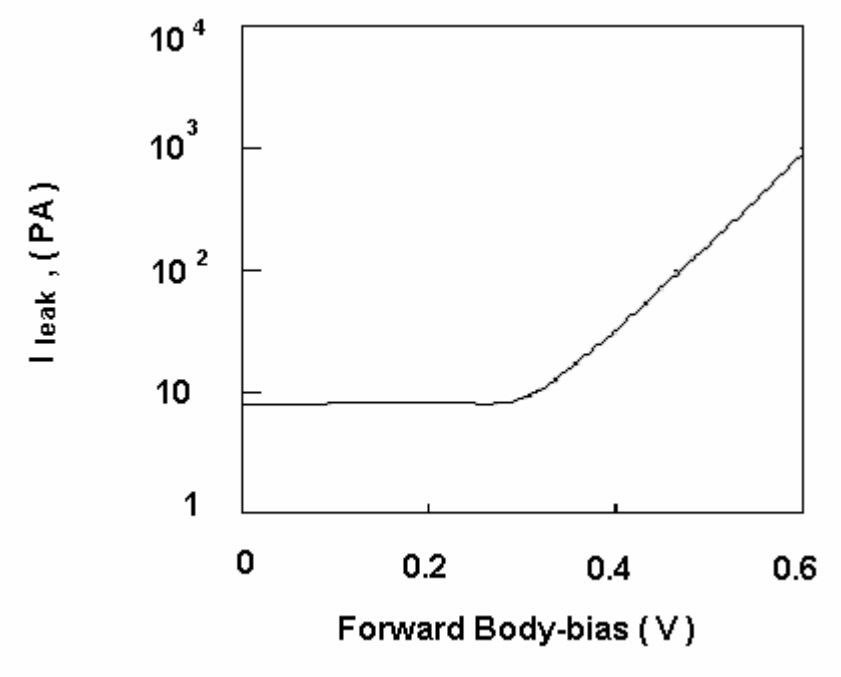


Figure 4.1: SPICE simulated leakage current of a CMOS inverter with increasing forward body-bias on n- and p-MOSFETs.

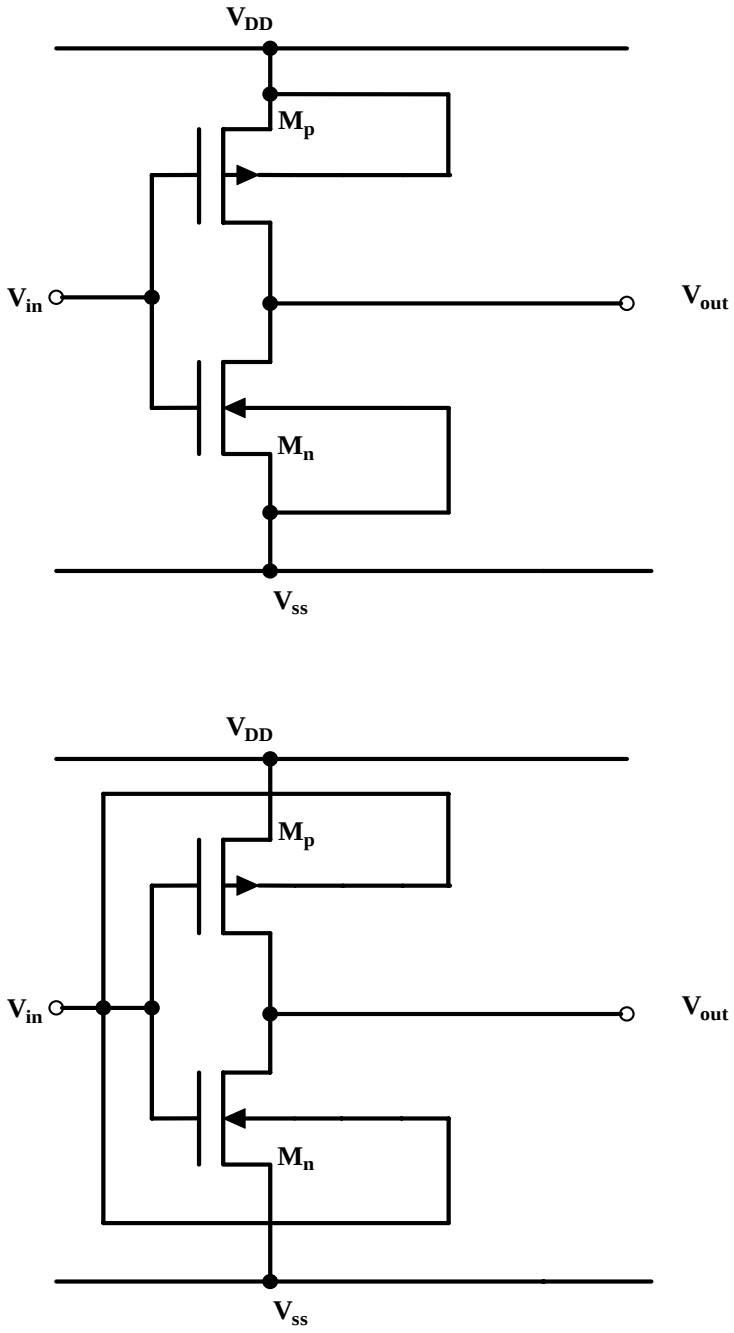


Figure 4.2: (a) Circuit diagram of a CMOS inverter, (b) Circuit diagram of a DTMOS inverter.

4.1 Improved DTMOS Inverter

Figure 4.3 shows a low voltage improved dynamic threshold MOS (DTMOS) inverter design which is combined with the forward body bias MOSFET. The conventional DTMOS [12] inverter is limited to its operation below 0.6 V since higher supply voltage will cause the forward body-bias greater than 0.6 V and then turn on the p-n junction between the source and the substrate. This poses a major limitation to the designer which has been showed as follows in Figure 4.3.

In Figure 4.3, the input is connected to the substrates of n-MOSFET and p-MOSFET through $M_{n,bias}$ and $M_{p,\ bias}$ where $M_{n,bias}$ and $M_{p,\ bias}$ act like the level shift transistors. The voltages applied to the substrate are limited by these transistors and are given by

$$V_{1,\min} = V_{bias,p} + |V_{TP}|, \text{ and} \tag{4.1}$$

$$V_{2,\max} = V_{bias,n} - |V_{TN}|. \tag{4.2}$$

Here $V_{1,min}$ and $V_{2,max}$ are minimum and maximum voltages which can be applied to bodies of n- and p-MOSFET in Fig. 4.3.

In this design, $|V_{TP}|$ is 0.6 V and V_{TN} is 0.5 V. A voltage of -0.6 V is applied to gate of $M_{p,\ bias}$. A voltage of 0.5 V is applied to gate of $M_{n,\ bias}$. $V_{1,\ min}$ is 0 V and $V_{2,\ max}$ is 0 V. The gate voltages ($V_{bias,\ p}$ and $V_{bias,\ n}$) of two transistors limit the transferred voltage (V_1 switches from 0 V to 0.4 V; V_2 switches from -0.4 V to 0 V), thus limit the forward body bias to be below 0.4 V. The $M_{p,\ bias}$ works as follows. The voltage at the right of $M_{p,bias}$ can swing from + 0.4 V to - 0.4 V. When the input voltage is + 0.4 V, it can go through $M_{p,\ bias}$ and apply to V_1. When input voltage decreases to 0 V, it still can go through $M_{p,\ bias}$ where the source-gate voltage across $M_{p,\ bias}$ is $|V_{TP}|$. When input voltage

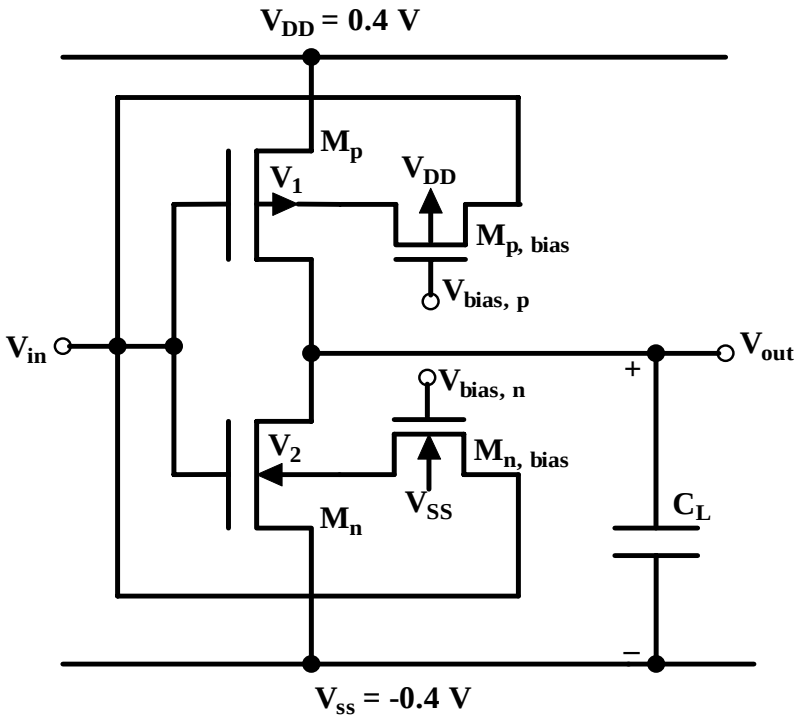


Figure 4.3: A CMOS inverter design using a switched-bias technique. W = 4.8 µm, L = 2.4 µm for M_n, W = 9.6 µm, L = 2.4 µm for M_p, W = 4.8 µm, L = 2.4 µm for $M_{n, bias}$, W = 9.6 µm, L = 2.4 µm for $M_{p, bias}$ and C_L = 1 fF. $V_{bias, p}$ = 0.6 V, $V_{bias, n}$ = 0.5 V, $|V_{TP}|$ = 0.6 V, V_{TN} = 0.5 V.

drops below 0 V, the source-gate voltage across $M_{p,\,bias}$ is less than $|V_{TP}|$. The $M_{p,\,bias}$ is off to prevent V_1 from going lower than 0 V. When input voltage drops below 0 V, the body-effect will make the threshold voltage of $M_{p,\,bias}$ higher which also help turn off the $M_{p,\,bias}$. The similar discussion also applies to the $M_{n,\,bias}$. In Fig. 4.3, V_{DD} and V_{SS} are ±0.4 V, respectively. Figure 4.4 shows the SPICE simulated input and output waveforms of a CMOS inverter using the improved dynamic body-bias technique of the circuit of Fig. 4.3. When the input voltage, V_{in} is high (+0.4 V), the source-substrate of n-MOSFET (M_n) is 0.4 V forward-biased and body of p-MOSFET is zero-biased. When V_{in} is low (-0.4 V), the source-substrate of p-MOSFET is 0.4 V forward-biased and body of n-MOSFET is zero-biased.

The dynamic body-bias technique has been used to design a CMOS analog multiplexer and a low voltage Schmitt trigger circuits for many applications. The design, simulation and experimental results of these CMOS circuits are presented in this chapter.

4.2 A Low Voltage Analog Multiplexer Design Using DTMOS Technique

The analog multiplexer in an integrated sensor connects the signal from a sensor to appropriate signal processing units such as the op-amp or analog-to-digital converter. Thus the multiplexer plays an important role to select and transfer a signal from the multi-channel signals. With proliferation of integrated sensors on a chip, low power analog multiplexer is extremely desirable. Use of such circuits efficiently reduce the power consumption and provides a long operation time. Integrating multiplexer and sensor on a chip will also reduce external noise, signal distortion and improve the system performance. In this work, a dynamic body bias switch is proposed to vary the threshold voltage at different operation modes. The dynamic body bias features following two

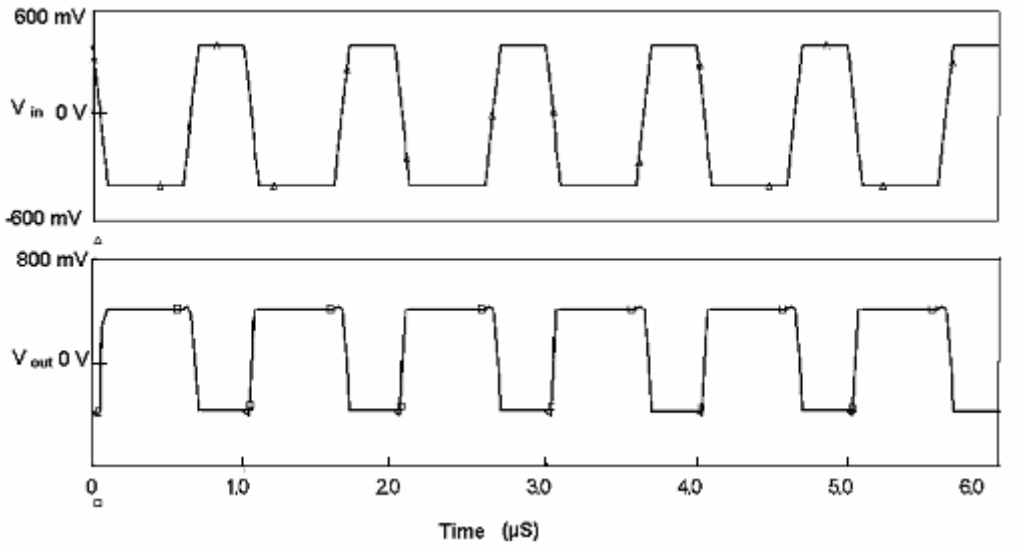


Figure 4.4: SPICE simulated performance a 0.8 V CMOS inverter using the dynamic body-bias technique.

modes: the forward body bias and the reverse body bias. The forward body bias reduces the operating voltage when the switch is in the "on" state. The reverse body bias lowers the signal leakage when the switch is in the "off" state. The leakage-to-signal ratio less than -120 dB can be achieved by using the dynamic bias technique. A 0.8 V low voltage CMOS multiplexer circuit is designed by combining a low voltage CMOS inverter with a low voltage CMOS switch. The proposed low voltage, low power CMOS analog multiplexer will find applications such as in on-chip neural microprobes integration with the low power CMOS amplifier [17] and other applications.

Figure 4.5 shows the block diagram of a 2-input analog multiplexer design. The multiplexer consists of an inverter and two switches, S_1 and S_2. When the switch, S_1 is closed and the switch, S_2 is open, the channel with the input, V_{in1} is selected. Similarly when the switch, S_2 is closed and the switch, S_1 is open, the channel with the input, V_{in2} is selected.

Figure 4.6 shows a CMOS switch design using the dynamic body-bias technique. V_{DD} and V_{SS} are ±0.4 V, respectively. The body bias is provided directly by the gate voltage. When the gate voltage, ϕ_1 is "high" (ϕ_2 is "low"), the body bias of n-MOSFET is V_{DD} and body bias of p-MOSFET is V_{SS}. The source-substrate junctions of both the transistors are forward biased. The transmission gate is "on". When ϕ_1 is "low" (ϕ_2 is "high"), the body bias of n-MOSFET is switched to V_{SS} and p-MOSFET switched to V_{DD}. The source-substrate junctions of both the transistors are reverse biased. The transmission gate is fully "off". Figure 4.7 shows the SPICE simulation of the switched-bias CMOS transmission gate shown in Fig. 4.6. It is shown in Fig. 4.7 that when the transmission gate is "on" from 0 μS to 10 μS, 1 mV sine wave input is transmitted to the

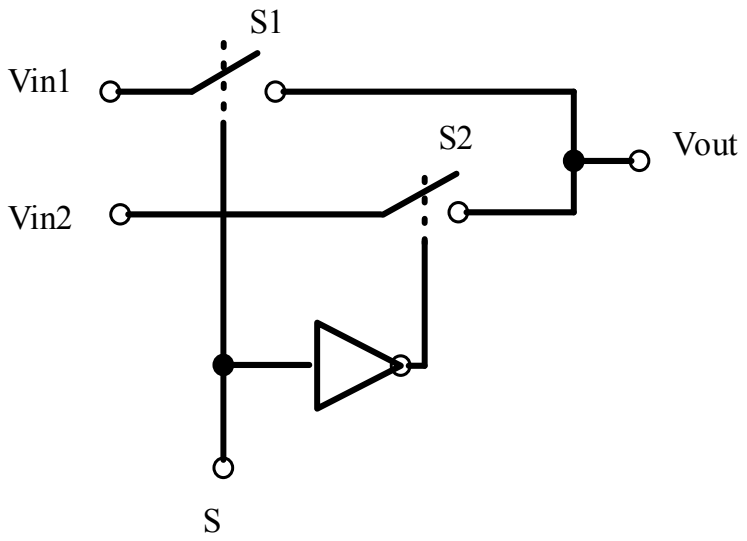


Figure 4.5: Block diagram of a 2-input analog multiplexer design.

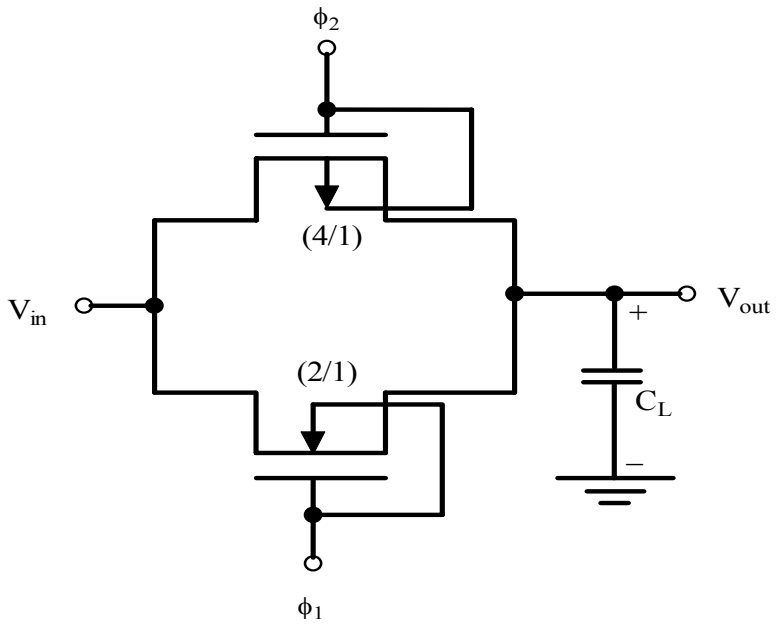


Figure 4.6: A CMOS switch design using the dynamic body-bias technique.

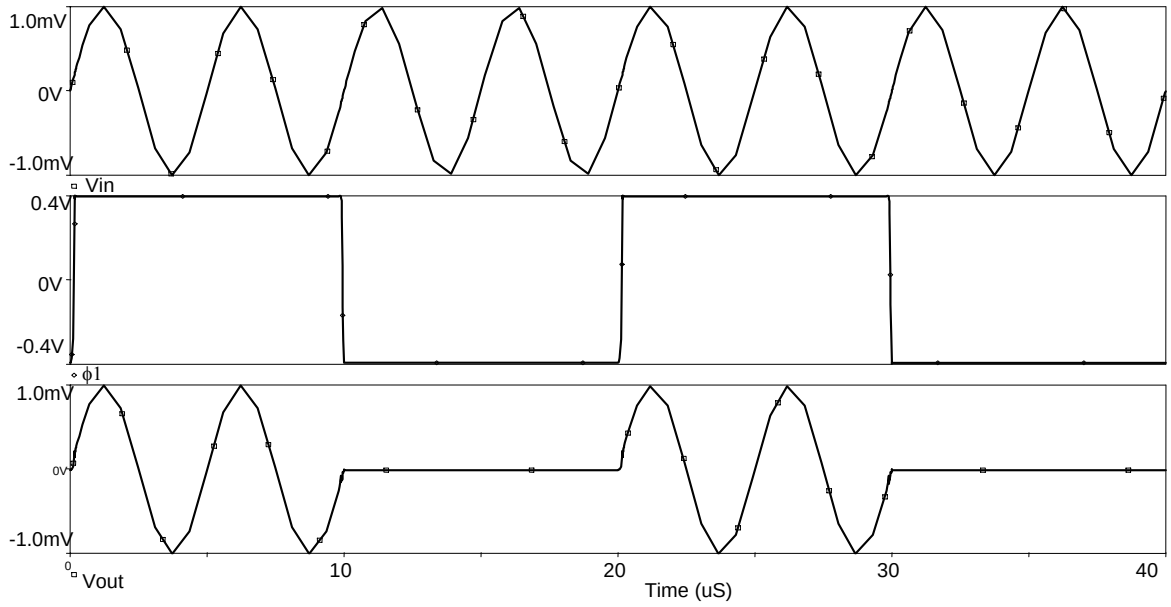


Figure 4.7: SPICE simulated dynamic body-bias transmission gate. The clock (ϕ_1) frequency is 50 kHz.

output. When the transmission gate is "off" from 10 μS to 20 μS, the input is on hold. The leakage signal is less than 2 nV. The leakage-to-signal ratio is less than -120 dB. Without switched-biased transistors, the leakage-to-signal ratio is as high as -40 dB or 2 μV.

The circuit diagram of an analog multiplexer using the dynamic body-bias technique is shown in Fig. 4.8 which includes switches and an inverter. The switches consist of p-MOSFETs only because the designed multiplexer circuit is for transferring small voltage signals which do not require full transmission gates. Figure 4.9 shows the post-layout SPICE simulated results. When control-S is '0', v_{in1} is transferred to the output of the multiplexer. When control-S is high, v_{in2} is transferred to the output. The total power consumption of analog multiplexer is 70 nW. The signal-to-leakage ratio is 120 dB. Figure 4.10 shows the waveforms of a 0.8 V improved DTMOS inverter circuit of Figure 4.8. The forward body bias is under 0.4 V. Figure 4.11 shows the measured response of the dynamic body-bias switch shown in Figure 4.8.

4.3 Low Voltage CMOS Schmitt Trigger Integrated Circuits

Schmitt trigger circuits are widely used for waveform shaping under noisy conditions in electronic circuits [36, 37]. In VLSI circuits, they are often used at chip input side and as single-ended receivers in DRAMs [38, 39]. The hysteresis in a Schmitt trigger circuit offers a better noise margin and noise stable operation. In a recent work [40], a low power Schmitt trigger circuit design is reported for 3 V operation. The cascade architecture used in this design limits the operation voltage. In this chapter, two novel CMOS Schmitt trigger circuits design are presented which use the dynamic body-bias method [12]. The first circuit is designed for operation at 1 V. The second circuit,

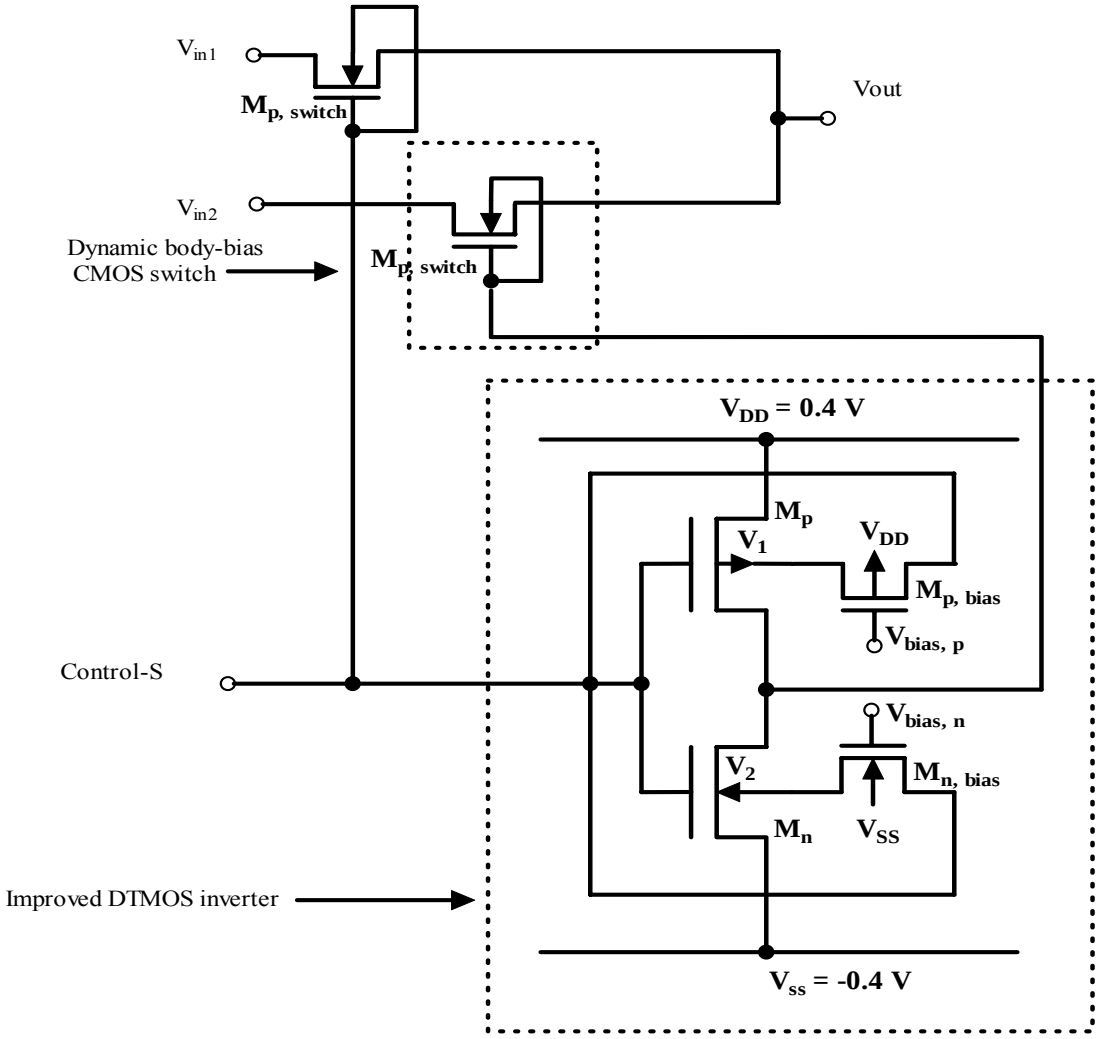


Figure 4.8: CMOS circuit diagram of a 2-input analog multiplexer using the dynamic body-bias technique. W = 9.6 µm, L = 2.4 µm for $M_{p, switch}$, W = 4.8 µm, L = 2.4 µm for M_n, W = 9.6 µm, L = 2.4 µm for M_p, W = 4.8 µm, L = 2.4 µm for $M_{n, bias}$, W = 9.6 µm, L = 2.4 µm for $M_{p, bias}$, $V_{bias, p}$ = 0.6 V, $V_{bias, n}$ = 0.5 V, $|V_{TP}|$ = 0.6 V and V_{TN} = 0.5 V.

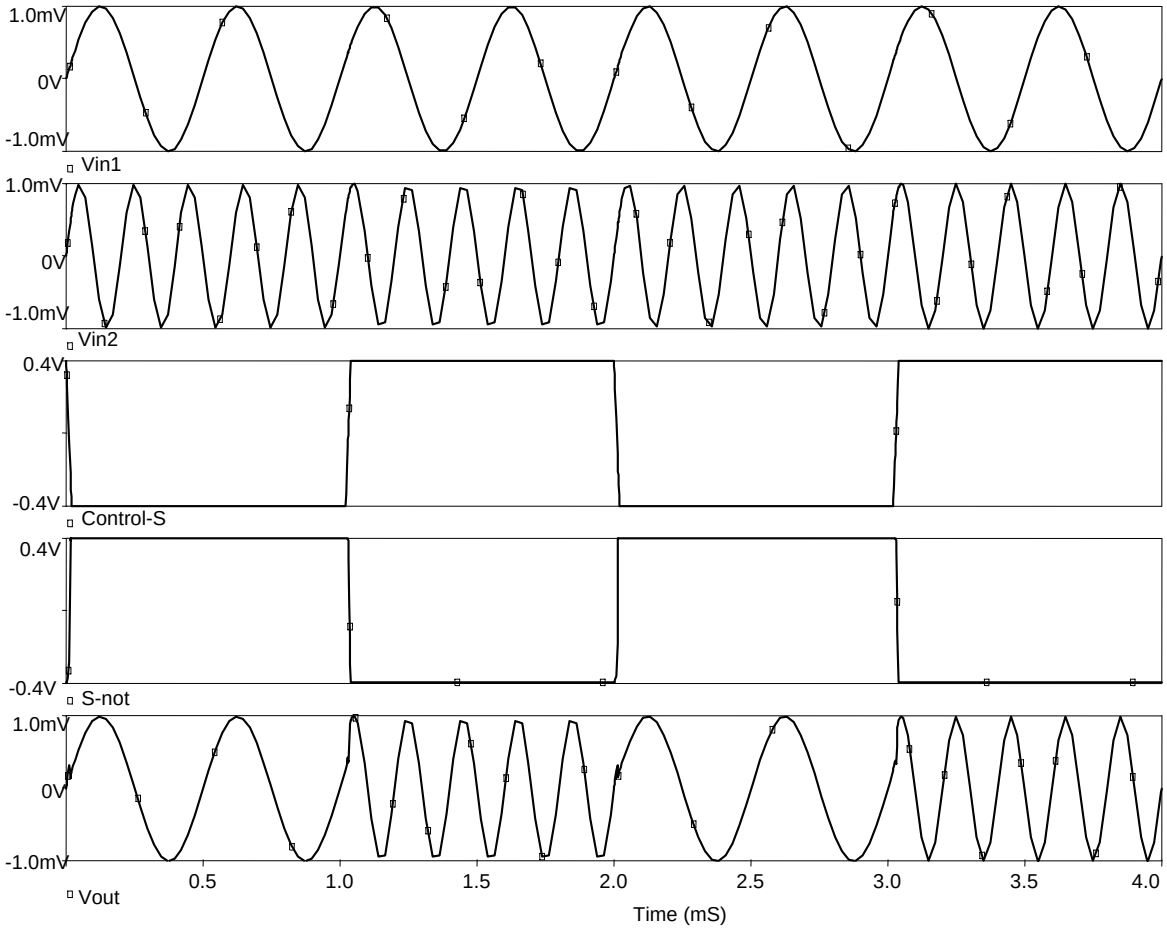


Figure 4.9: SPICE simulated input and output waveforms of a 0.8 V analog multiplexer.

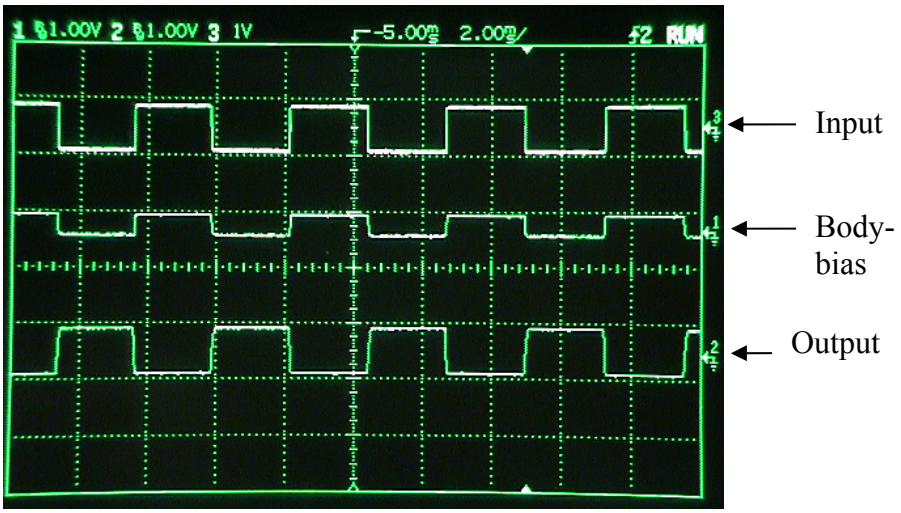


Figure 4.10: Measured waveforms of a 0.8 V DTMOS inverter. Scale: X-axis: 2mS/div, Y-axis: 1 V/div.

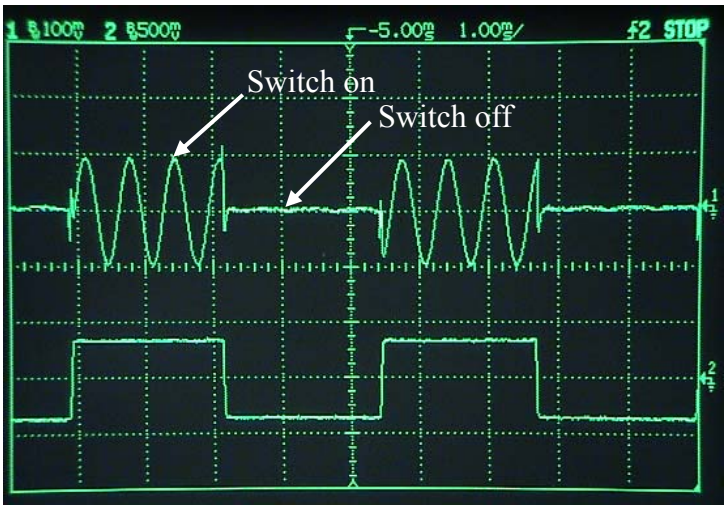


Figure 4.11: Measured behavior of a ± 0.4 V CMOS switch. Scale: X-axis: 1mS/div, Y-axis: 0.5 V/div.

derived from the first circuit, is designed for operation at 0.4 V. Experimental results for the new Schmitt trigger circuits are presented.

The standard CMOS Schmitt trigger circuit design [1] is shown in the Fig. 4.12. The operation of the Schmitt trigger circuit is as follows. Initially, V_{in} = 0 V, the two stacked p-MOSFET (M_{p1} and M_{p2}) will be on. Hence $V_{out1} = V_{DD}$. When V_{in} rises to V_{TN}, M_{n2} is on. But M_{n1} is still off since M_{n3} is on and source voltage of M_{n1} is V_{DD}. Now M_{n2} and M_{n3} form an inverting n-MOS amplifier. Thus, source voltage of M_{n1} is falling with increasing V_{in}. When source voltage of M_{n1} drops to V_{TN}, M_{n1} is on. Now both M_{n1} and M_{n2} are on, V_{out1} approaches to 0 V rapidly and M_{n3} becomes off. When V_{in} approaches V_{DD}, the two stacked n-MOSFET (M_{n1} and M_{n2}) will be on. Hence V_{out1} = 0. When V_{in} falls to $|V_{TP}|$, M_{p2} is on. But M_{p1} is still off since M_{p3} is on and source voltage of M_{p1} is 0 V. Now M_{p2} and M_{p3} form an inverting p-MOS amplifier. Thus, source voltage of M_{p1} is rising with decreasing V_{in}. When source voltage of M_{p1} rises to $|V_{TP}|$, M_{p1} is on. Now both M_{p1} and M_{p2} are on, V_{out1} approaches to V_{DD} rapidly and M_{p3} becomes off. The voltage transfers characteristic exhibits a typical hysteresis behavior as shown in Fig. 4.13.

In Figure 4.13, V_{OH} is the maximum output voltage and V_{OL} is the minimum output voltage. V_{hl} is the input voltage at which output switches from V_{OH} to V_{OL}. V_{lh} is the input voltage at which output switches from V_{OL} to V_{OH}. V_{hw} is called the hysteresis width. The voltages, V_{hl}, V_{lh} and V_{hw} are given by [1]

$$V_{hl} = \frac{V_{DD} + RV_{TN}}{R+1}, \tag{4.3}$$

$$V_{lh} = \frac{R|V_{TP}|}{R+1} \text{ and} \tag{4.4}$$

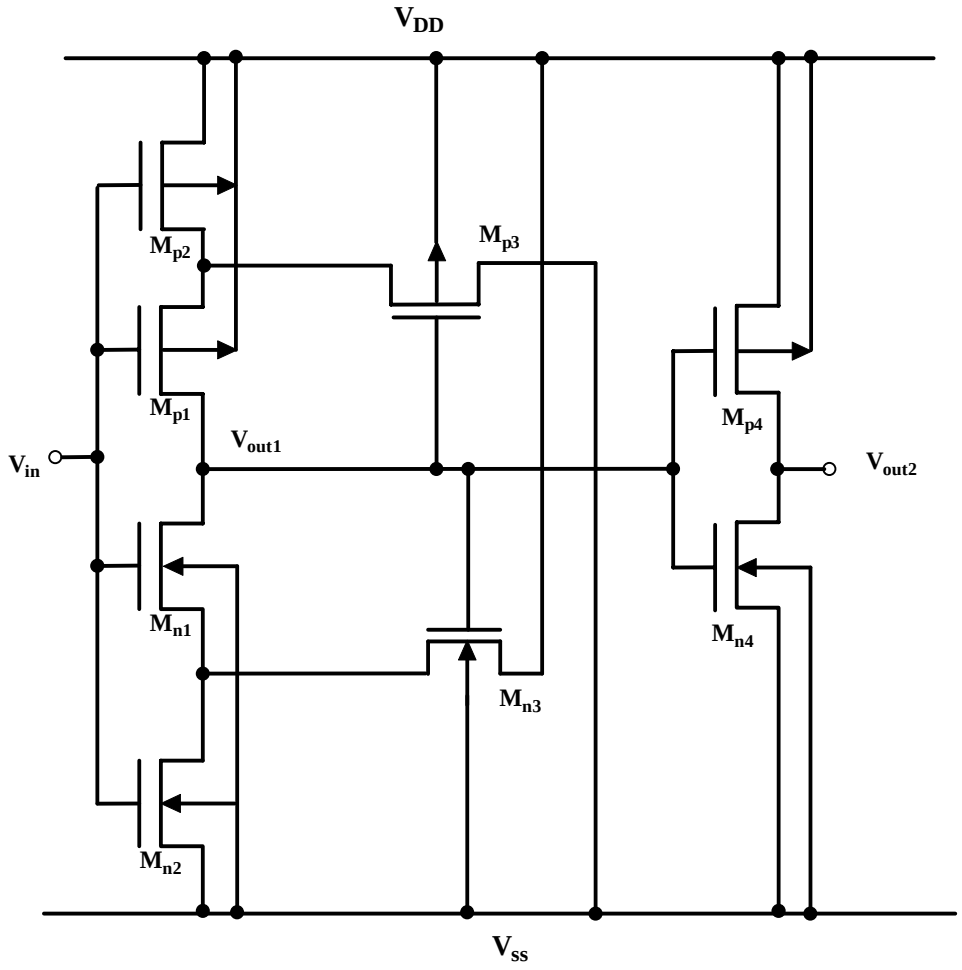


Figure 4.12: A standard CMOS Schmitt trigger circuit design.

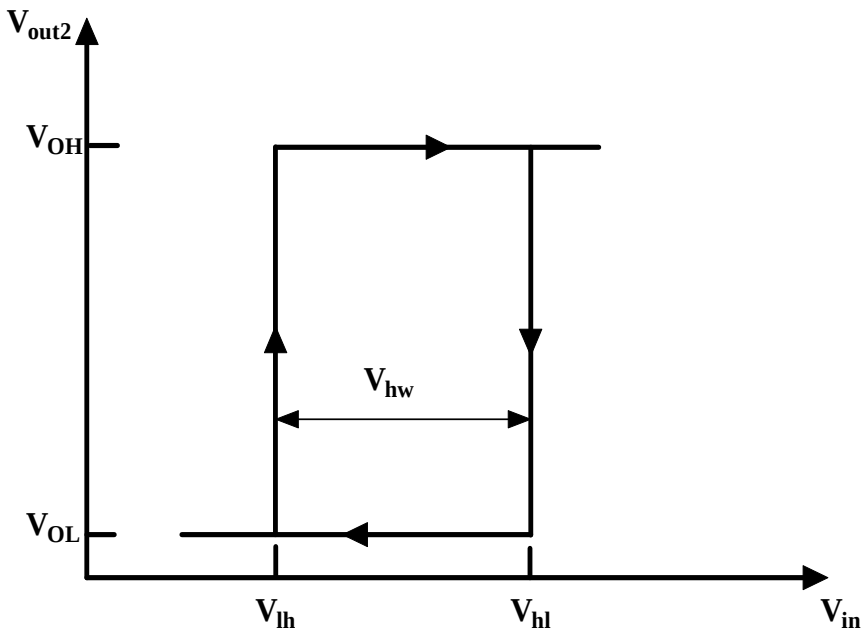


Figure 4.13: CMOS Schmitt trigger voltage transfer characteristic.

$$V_{hw} = V_{hl} - V_{lh} = \frac{V_{DD} + R(V_{TN} - |V_{TP}|)}{R+1} \tag{4.5}$$

where the ratio $R = \sqrt{\beta_n / \beta_p}$. The n- and p-MOSFETs' transconductance parameters are β_n and β_p, respectively.

The cascade architecture used in the CMOS Schmitt trigger circuit design of Fig. 4.12 limits lowering of the operating voltage. In the following section, we describe novel Schmitt trigger circuits designs in CMOS for operation at 1 V or lower using a dynamic body-bias method [12].

Figure 4.14 shows the proposed 1 V Schmitt trigger circuit [23]. In this design, a dynamic body-bias is applied to a simple CMOS inverter circuit, whereby the threshold voltages of the two MOSFETs can be changed therteby changing the switching voltage. The operation of the circuit of Fig. 4.14 can be described as follows. First, the values of bias voltages $V_{bias,p}$ and $V_{bias,n}$ are respectively set externally to values (-|V_{TP3}|+ 0.1) V and (V_{TN3} – 0.1) V. This ensures that the drain voltage magnitudes of the MOSFETs, M_{p3} and M_{n3} and hence body voltage magnitudes of the MOSFETs M_{p1} and M_{n1} will have a value of +0.1 V minimum, and –0.1 V maximum, respectively when the transistor is conducting. This will limit forward body-bias in transistors M_{n1} and M_{p1} to 0.4 V. A forward bias greater than 0.4 V may trigger latchup in a CMOS circuit [15]. When a low value signal is applied to V_{in}, V_{out2} goes low. V_{out2} provides zero forward body-bias to the transistors of M_{n1} through M_{n3} operating in linear region and a forward bias of 0.4 V to M_{p1} through M_{p3} operating in saturation region. The substrate of transistor M_{n1} is biased at -0.5 V and its threshold voltage now corresponds to the value at zero substrate bias, V_{TNO1}, while the substrate of transistor M_{p1} is biased at +0.1 V with its threshold voltage

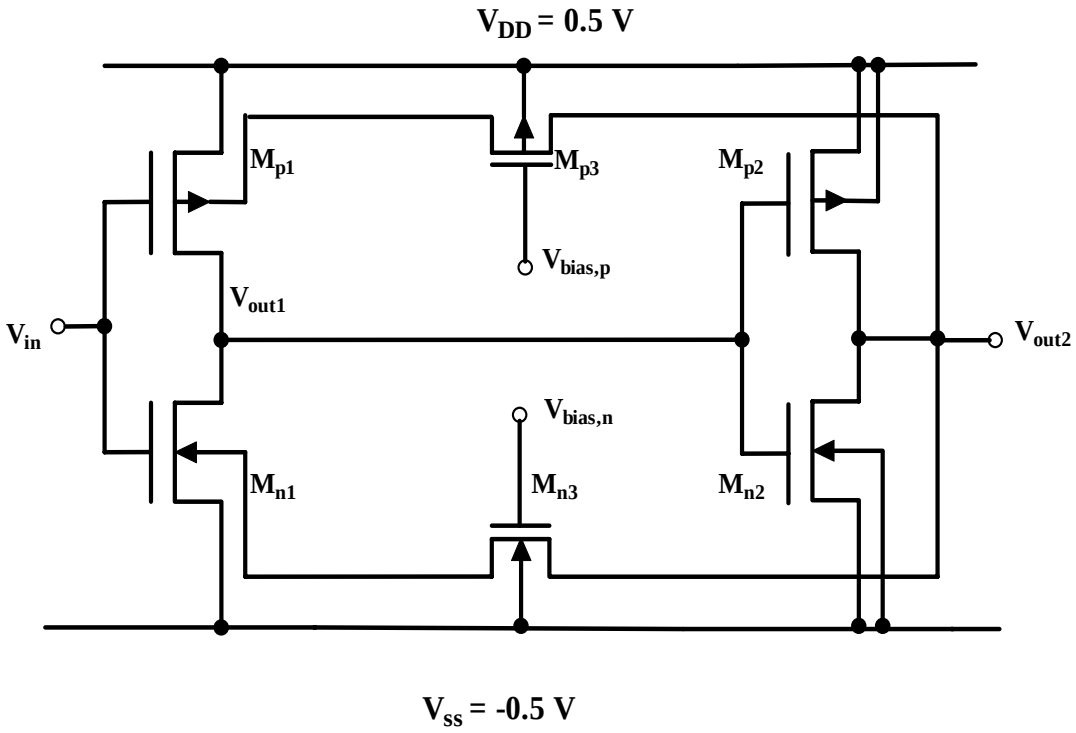


Figure 4.14: Proposed 1-V Schmitt trigger design [23].

corresponding to +0.4 V forward-bias value, $|V_{TP1}|$.

Transistor M_{p1} remains on and M_{n1} remains off until V_{in} increases to a certain voltage V_{hl}, at which output, V_{out1} switches from a high to a low value and V_{out2} switches from a low to a high value. Since M_{n1} substrate is at zero body bias, its threshold voltage V_{TNO1} is higher than the value for the forward body bias. Hence, a higher voltage is needed to turn M_{n1} on. For a ramp input, this results in a time delay t_1, as V_{out1} goes to a low value and V_{out2} goes to a high value of V_{DD}. This provides a 0.4 V forward body bias to M_{n1} through the transistor M_{n3} operating in saturation at the end of the switching transient period. A zero body bias is now provided to M_{p1} through the transistor M_{p3} operating in linear region at the end of the switching transient. Transistor M_{p1} is now off and M_{n1} remain on until V_{in} decreases to a certain voltage V_{lh}, at which output, V_{out1} switches from low to high and V_{out2} switches from high to low. Since M_{n1} has forward substrate body bias, a lower voltage is now needed to turn it off. This results in a time delay t_2 for a ramp input. The different switching voltage or switching time causes the hystersis. V_{out1} is buffered by M_{p2}-M_{n2} inverter, which provides high fan-out capability. Thus, output is taken at V_{out2} terminal.

The switching voltage V_{hl} can be calculated using following equations:

$$\frac{\beta_n}{2}\left(V_{hl}-V_{TNO}\right)^2=\frac{\beta_p}{2}\left(V_{DD}-V_{hl}-|V_{TP}|\right)^2 \tag{4.6}$$

and

$$V_{hl}=\frac{V_{DD}-|V_{TP}|+RV_{TNO}}{R+1}. \tag{4.7}$$

V_{TNO} is the zero substrate body bias threshold voltage of n-MOSFET, V_{TP} is forward substrate body bias threshold voltage of p-MOSFET, and V_{DD} is the supply voltage.

A similar analysis can be used to calculate V_{lh} and is given by

$$V_{lh} = \frac{V_{DD} + RV_{TN} - |V_{TPO}|}{R+1} \tag{4.8}$$

where V_{TN} is the forward substrate body bias threshold voltage of the n-MOSFET, $|V_{TPO}|$ is the zero substrate body bias threshold voltage of the p-MOSFET. The hysteresis width, V_{hw} is then calculated as follows:

$$V_{hw} = V_{hl} - V_{lh} = \frac{(|V_{TPO}| - |V_{TP}|) + R(V_{TNO} - V_{TN})}{R+1}. \tag{4.9}$$

Figure 4.15 shows a CMOS Schmitt trigger circuit design for operation at an extreme low voltage value of 0.4 V. The configuration of Fig. 4.15 does not allow the forward body-bias to exceed 0.4 V. Thus, the transistors M_{p3} and M_{n3} shown in the circuit of Fig. 4.14 are not required in the circuit of Fig. 4.15. The configuration of M_{p2} and M_{n2} is called dynamic threshold MOS (DTMOS) [1] inverter that ensures the inverter operation at ultra-low voltage of 0.4 V. The trigger operation of Fig. 4.15 can be described as follows. When a low value signal is applied to V_{in}, V_{out2} goes low. V_{out2} provides zero forward body-bias to the transistors of M_{n1} and a forward bias of 0.4 V to M_{p1}. The substrate of transistor M_{n1} is biased at -0.2 V and its threshold voltage now corresponds to the value at zero substrate bias, V_{TNO1}, while the substrate of transistor M_{p1} is biased at -0.2 V with its threshold voltage corresponding to +0.4 V forward-bias value, $|V_{TP1}|$. Transistor M_{p1} remains on and M_{n1} remains off until V_{in} increases to a certain voltage V_{hl}, at which output, V_{out1} switches from a high to a low value and V_{out2} switches from a low to a high value. Since M_{n1} substrate is at zero body bias, its threshold voltage V_{TNO1} is higher than the value for the forward body bias. Hence, a higher voltage is needed to turn M_{n1} on. For a ramp input, this results in a time delay t_1, as V_{out1} goes to a low value and V_{out2} goes to a high value of V_{DD}. This provides a 0.4 V forward body

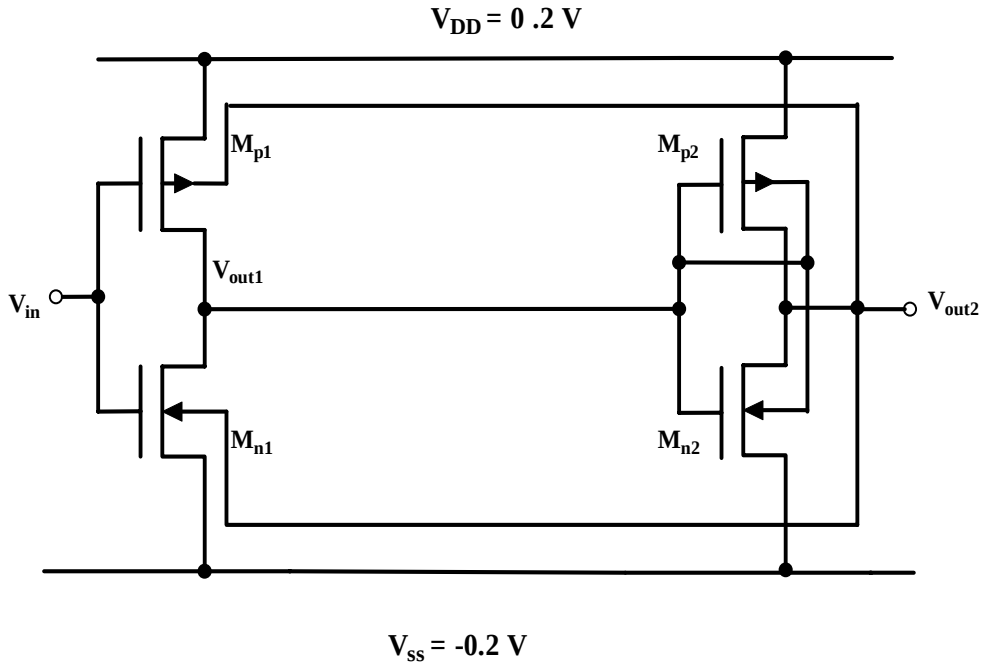


Figure 4.15: A 0.4 V CMOS Schmitt trigger circuit derived from Figure 4.14 [23].

bias to M_{n1} at the end of the switching transient period. A zero body bias is now provided to M_{p1} at the end of the switching transient. Transistor M_{p1} is now off and M_{n1} remain on until V_{in} decreases to a certain voltage V_{lh}, at which output, V_{out1} switches from low to high and V_{out2} switches from high to low. Since M_{n1} has forward substrate body bias, a lower voltage is now needed to turn it off. This results in a time delay t_2 for a ramp input. The different switching voltage or switching time causes the hystersis. V_{out1} is buffered by M_{p2}-M_{n2} inverter, which provides high fan-out capability. Thus, output is taken at V_{out2} terminal. It is shown in Fig. 4.16 that V_{out1} has a slow transition but V_{out2} has a fast transition.

Figure 4.17 (a) and (b) show the measured hysterisis and input-output characteristics of a CMOS Schmitt trigger implemented in standard 1.5 μm CMOS process corresponding to circuit of Fig. 4.14. Figures 4.18 (a) and (b) show similar characteristics for the circuit of Fig. 4.15. The measured hysterisis width, V_{hw}, is close 0.15 V for both Schmitt trigger circuits shown in Fig. 4.14 and 4.15 and agrees with the corresponding calculated value of 0.15 V from Eq. 4.9, for 0.4 V forward body-bias and R=1.

4.4 Summary

Two low power circuits using improved DTMOS technique are presented. A 0.8 V low voltage analog multiplexer is designed. It can be integrated on a chip with sensors to connect low voltage signals such as biological or chemical signals with reduced noise and distortion. Dynamic-bias technique is applied to a sub-circuit design such as switches and inverters to reduce signal leakage while maintaining low voltage operation. An improved DTMOS configuration ensures the forward body bias below 0.4 V.

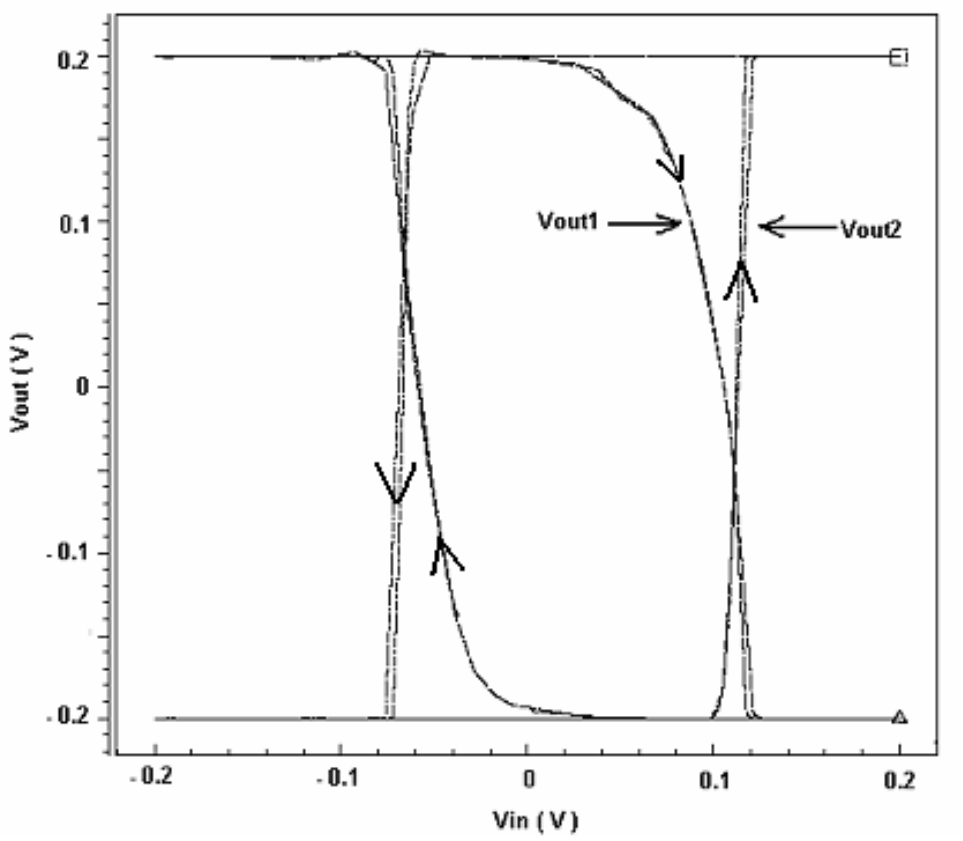
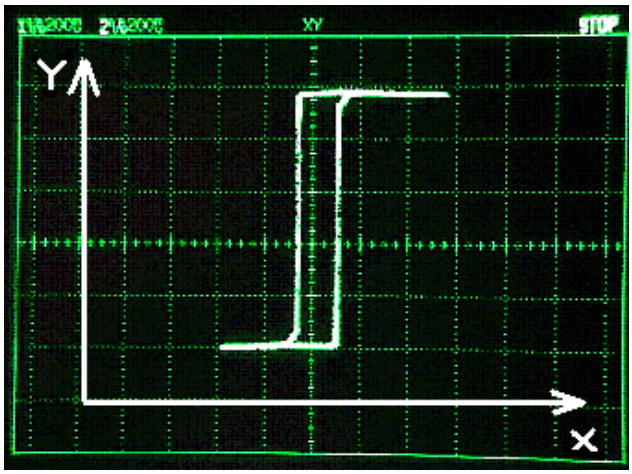
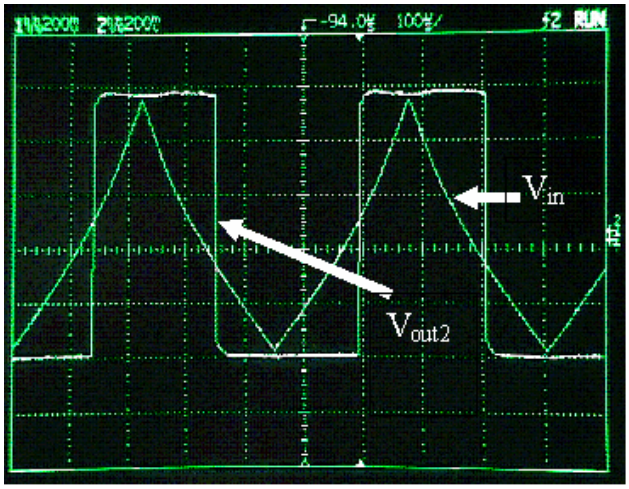


Figure 4.16: Simulated input-output (V_{in}-V_{out1} and V_{in}-V_{out2}) waveform characteristics of Schmitt trigger circuit shown in Fig. 4.15.

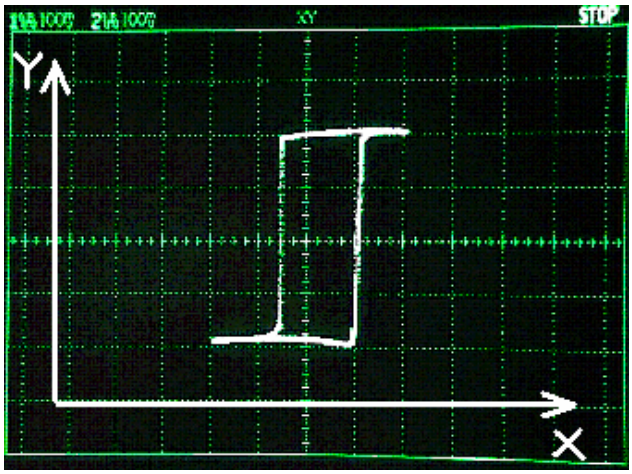


(a)

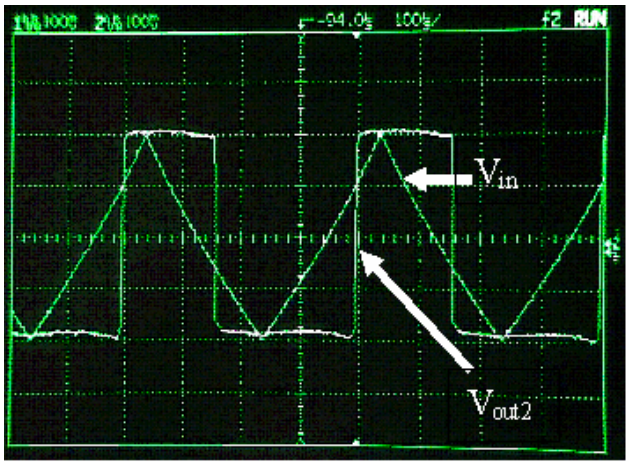


(b)

Figure 4.17: (a) Measured hysterisis characteristics (V_{out2} Versus V_{in}) of the 1 V CMOS Schmitt trigger circuit in Figure 4.14. X-axis is V_{in} and Y-axis is V_{out2}, (b) Measured input-output (V_{in}-V_{out2}) waveform characteristics.: X-axis = 0.2 V/div., Y-axis = 0.2 V/div., V_{in} = - 0.5 V to +0.5 V ramp.



(a)



(b)

Figure 4.18: (a) Measured hysterisis characteristic of the 0.4 V CMOS Schmitt trigger circuit in Figure 4.15. X-axis is V_{in} and Y-axis is V_{out2}, (b) Measured input-output (V_{in}-V_{out2}) waveform characteristics. X-axis = 0.1 V/div., Y-axis = 0.1 V/div., V_{in} = - 0.2 V to +0.2 V ramp.

. Two CMOS Schmitt trigger circuits have been implemented in standard 1.5 µm CMOS process for operation at 1 V and 0.4 V using the dynamic threshold technique. This method exploits lowering of the threshold voltage of a MOSFET under forward substrate body bias. Measured hysterisis widths agree closely with the corresponding calculated value of 0.15 V. The proposed CMOS Schmitt trigger circuits are extremely useful in low/ultra-low voltage circuit applications.

CHAPTER 5

ADAPTIVE BODY-BIAS GENERATOR CIRCUIT

The substrate (body) of a MOSFET has been the subject of intensive research since body-biasing conditions benefit the CMOS chip design for low power application [4, 12, 15, and 16]. Varying body-bias is a key method to vary the threshold voltage of a MOSFET. From the physics of MOS devices, forward body-bias is known to lower the threshold voltage of a MOSFET as we discussed in Chapter 2. The supply voltage can be reduced or operational frequency can be increased without lowering the system performance. However, the forward body-bias increases the leakage current which contributes significantly to power dissipation in high density chips. With the current trend of scaled down CMOS technology, therefore, reduction of leakage current in a MOSFET has become an important issue. A few approaches have been reported to reduce the leakage current in a MOSFET [4, 12] including the multi-threshold voltage process [4]. Low threshold MOSFETs are used in critical paths of a CMOS circuit design while high threshold MOSFETs are used in non-critical paths. Assaderaghi et al. [12] have proposed a dynamic threshold MOSFET in which body terminal is tied to the gate so that MOSFETs are forward body-biased when the transistor is ‘on’ and reverse biased when the transistor is ‘off’. In reverse body-bias condition, threshold voltage is increased, thus leakage current is reduced. This method was discussed and further improved in the Chapter 4.

However, methods described above have their disadvantages. The multi-threshold voltage process is not a cost effective process. On the other hand, dynamic threshold MOSFETs are limited to ultra-low voltage operation since forward body-bias above 0.4

V may turn on the P-N junction between the source and substrate and may cause CMOS latchup [15]. Improved DTMOS method though effective, doubles the number of transistors in design. An adaptive body-bias generator is highly desirable in varying the body-bias in CMOS circuit design. In this chapter, a simple adaptive body-bias technique is proposed. When high performance is not needed, reduction of leakage current is achieved by switching the body-bias from a forward-bias to a reverse-bias condition.

5.1 A CMOS Adaptive Body-Bias Generator Circuit Design

Figure 5.1 (a) shows the block diagram of an adaptive body-bias generator. Figure 5.1 (b) shows the logic diagram of its building blocks including 3-bit D-flip flop and 8-to-1 multiplexer. The 3-bit counter is implemented using master-slave J-K flip flops. The 8-to-1 multiplexer is implemented using CMOS switches (transmission gates). The 3–bit D-flip flops are designed using positive edge triggered J-K flip flops. A reference clock signal is needed to represent the system frequency. When the frequency of reference clock is set “high”, a forward body-bias is preferred. When the frequency of reference clock is set “low”, a reverse body-bias is preferred. Adaptive body-bias generator is designed in such a way that it can generate body-biases depending on operating conditions.

In Fig. 5.1, the ring oscillator generates a clock signal. The 3-bit counter counts when the reference clock goes low (“0”). When the reference clock goes high (“1”), data of the counters are stored in a 3-bit positive-edge triggered D-flip flop and then counter is reset to zero. The ring oscillator can be designed in such way so that the counter initially counts 3 pulses with the reference clock, f_o and $V_{bias,3}$ is selected through a 8-to-1

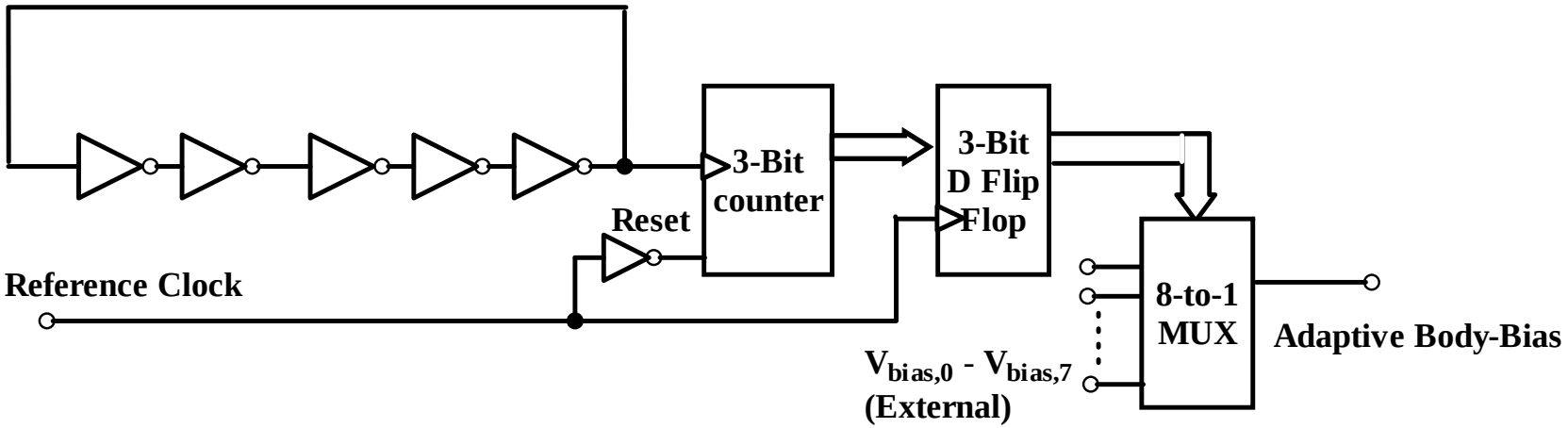
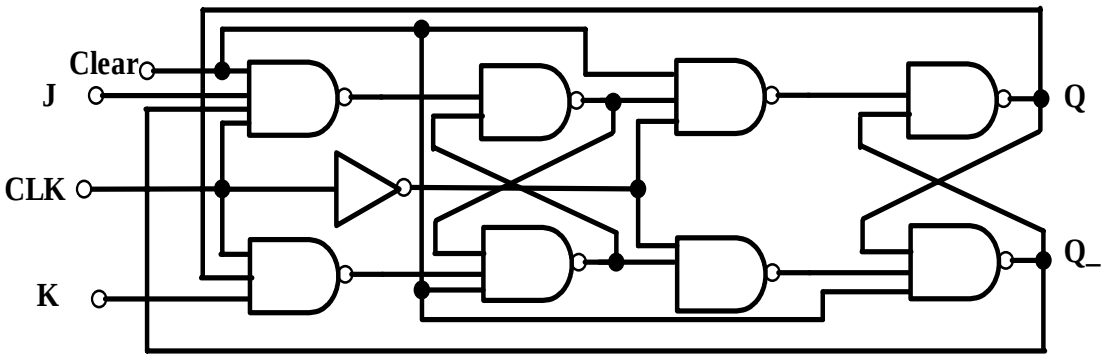
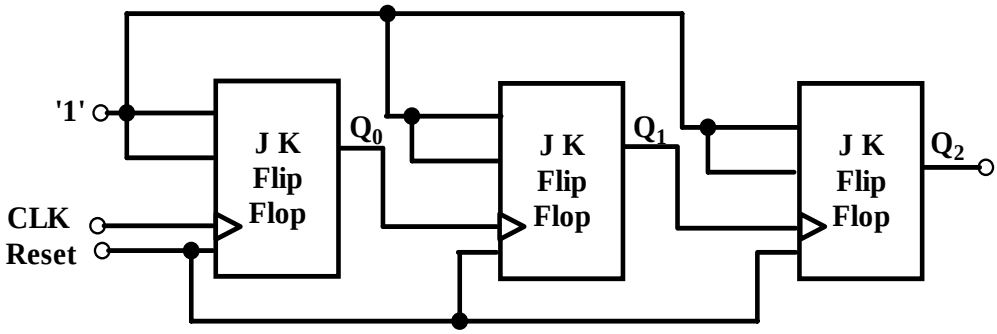


Figure 5.1: (a) Block diagram of an adaptive body-bias generator. V_{DD}=3.0 V and V_{SS}=0 V. (b) Master-slave JK flip flop, (c) 3-bit counter, (d) 3-bit D-flip flop and (e) 8-to-1 Multiplexer.

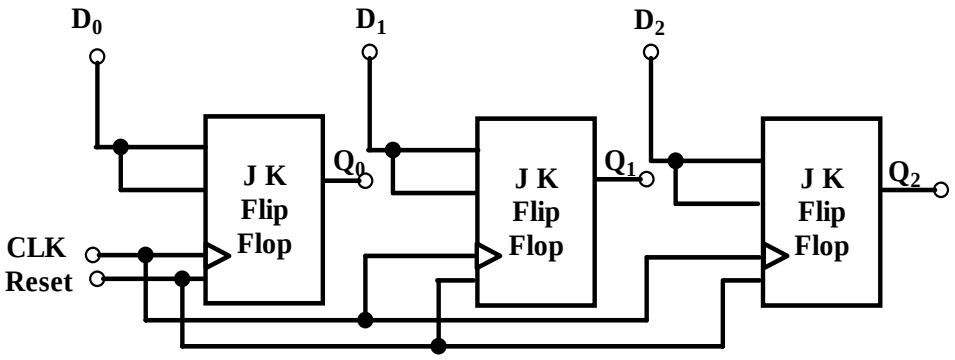


(b)



(c)

(Fig. 5.1 cont'd)



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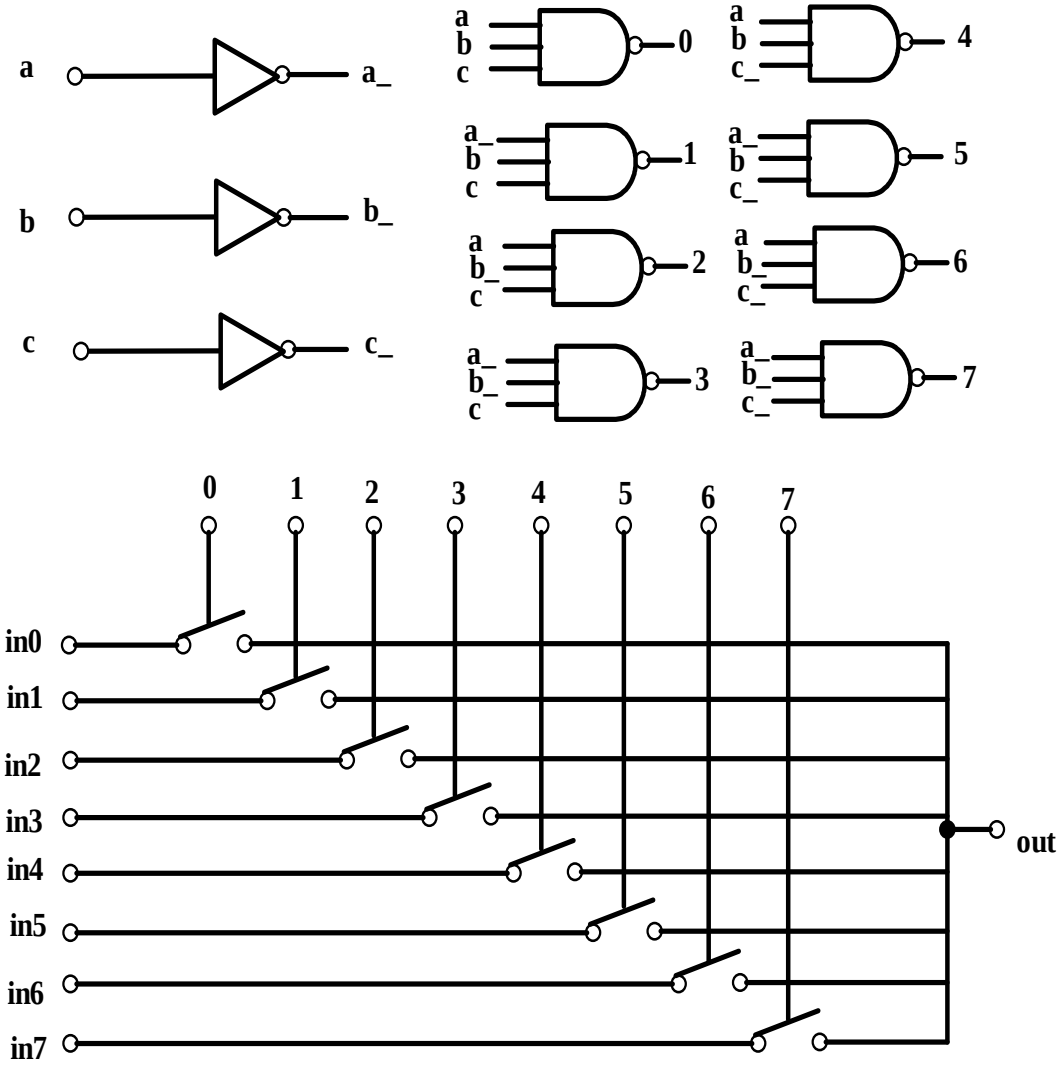

(e)

(Fig. 5.1 cont'd)

multiplexer where $V_{bias,3}$ is a zero-biased body voltage. There are 8 levels of body-biases, $V_{bias,0}$ to $V_{bias,7}$ and can be selected depending on the output of the D-flip flop. The 8-level binary body-biases, $V_{bias,0}$ to $V_{bias,7}$ vary from a forward body-bias of +0.3 V to a reverse body-bias of -0.4 V with a decrement of 0.1 V.

Initially zero body-bias, $V_{bias,3}$ is selected. With the increasing operational frequency which is given by the reference clock, counter counts less number of pulses and $V_{bias,2}$ to $V_{bias,0}$ may be selected. With decreasing operational frequency of the reference clock, counter counts more number of pulses and $V_{bias,4}$ to $V_{bias,7}$ may be selected to provide a reverse body-bias for lowering the leakage current. Table 5.1 shows truth table of the 8-to-1 multiplexer which generates body-bias for p-MOSFETs.

Fig. 5.2 shows an operational timing diagram of the adaptive body-bias generator circuit of Fig. 5.1. The clear signal has a time delay to ensure that the D-flip flop properly samples the counter output before the counter is cleared. The 3-bit counter is designed to count 000 to 111 and will keep 111 before being reset to zero. A regular 3-bit counter shown in Fig. 5.1 has been modified as shown in Fig. 5.3 to perform the counting function in Fig. 5.2. The counter in Fig. 5.3 counts from 000 to 111. Before output reaches 111, the select signal remains high ("1"). V_{out} from ring oscillator is selected to trigger the counter. When 3-bit output, V_{out} is 111, select signal is low ("0"). No clock triggers the counter since clock output from 2-to-1 MUX is "0" and 3-bit V_{out} remains at 111.

Figure 5.4 shows the measured adaptive body-bias versus reference clock frequency of a p-MOSFET. The 8-level body-bias varies from -0.3 V to +0.4 V with a 0.1 V increment. In the design, initially the counter counts 3 with f_o of 270 kHz.

Table 5.1. Truth table of an 8-to-1 multiplexer

Output of 3-bit D flip flop	**Output of multiplexer V_{bias}**	**V_{bias}**
000	$V_{bias,0}$	0.3V
001	$V_{bias,1}$	0.2V
010	$V_{bias,2}$	0.1V
011	$V_{bias,3}$	0V
100	$V_{bias,4}$	-0.1V
101	$V_{bias,5}$	-0.2V
110	$V_{bias,6}$	-0.3V
111	$V_{bias,7}$	-0.4 V

Note: A positive V_{bias} is a reverse body-bias; and a negative V_{bias} is forward body-bias. The actual voltage value applied to body terminal of p-MOSFET is $V_{DD}+V_{bias}$.

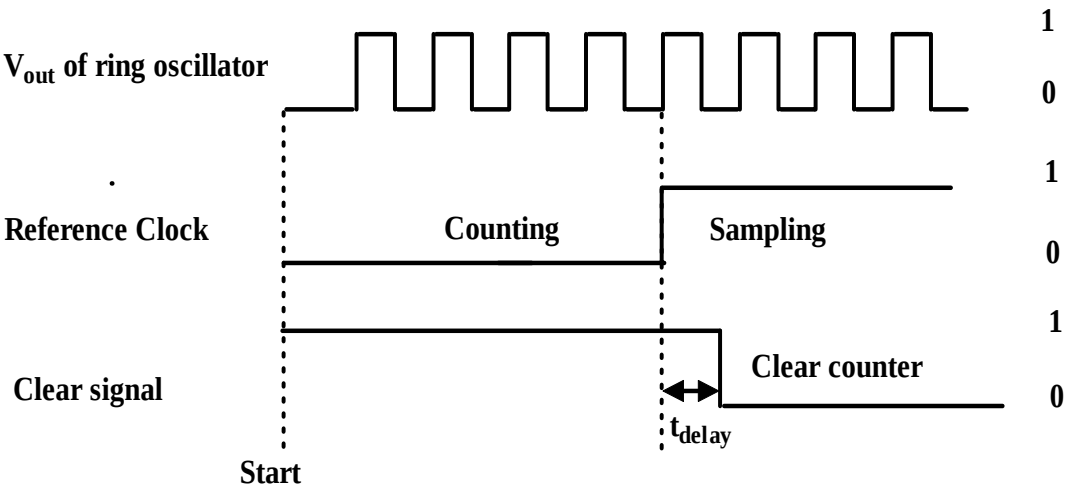

Figure 5.2: Operational timing diagram of the adaptive body-bias generator.

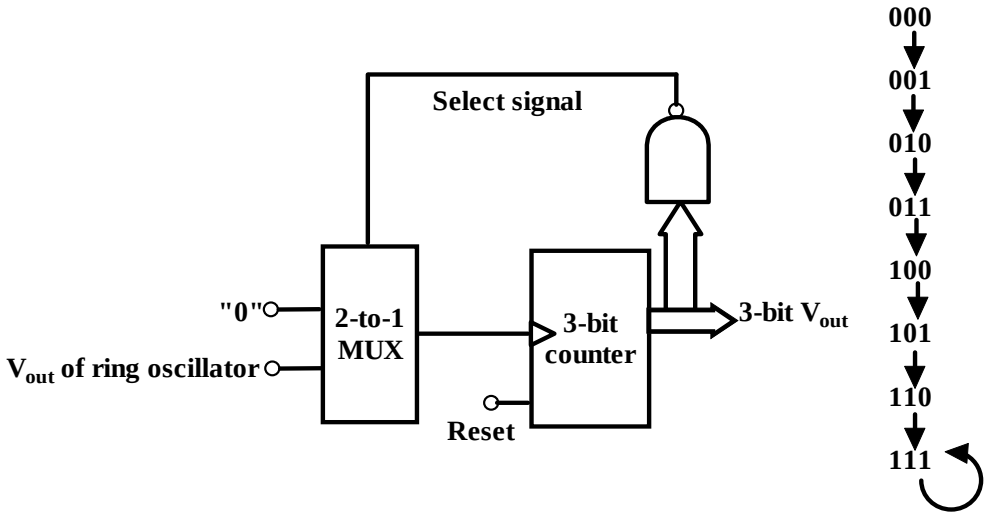

Figure 5.3: Logic diagram of a 3-bit counter design.

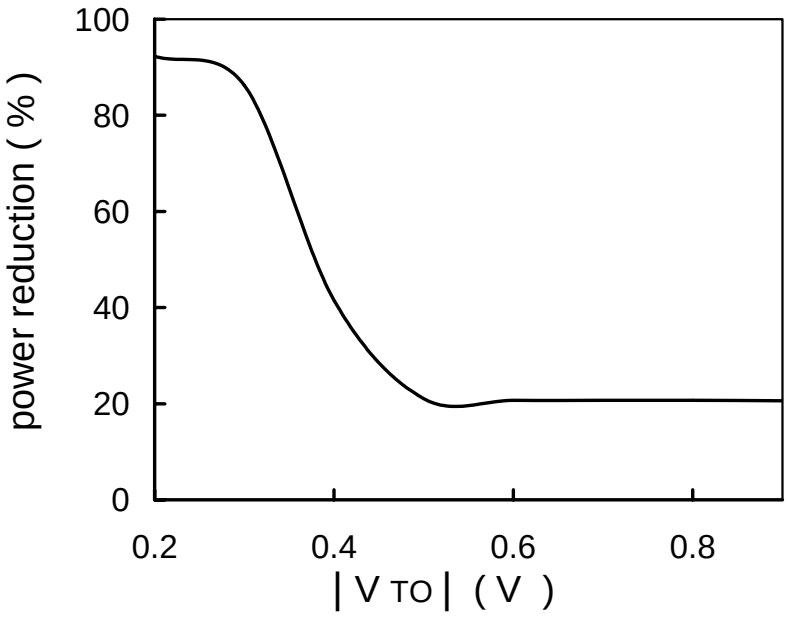

Figure 5.4: Body-bias of a p-MOSFET versus reference clock when initially $V_{bias,3} = 0V$ at 270 kHz and the counter counts 3.

5.2 Reduction of Leakage Current

In this section, factors which affect leakage current, such as the transistor size and threshold voltage are analyzed. A simple inverter consisting of an n-MOSFET and a p-MOSFET with zero-biased threshold voltage of -0.85 V for the p-MOSFET and 0.55 V for the n-MOSFET is used to simulate the leakage current. These are the values of a typical MOSIS 1.5 μm n-well CMOS process. The leakage current increases with increasing W/L ratio of transistors as shown in Fig. 5.5.

The body-bias output from the circuit of Fig. 5.1 has been applied to a p-MOSFET in Fig. 5.6 for illustration in leakage current reduction. In the present work, body-bias could be applied to a p-MOSFET only because single n-well process does not allow different forward-body bias to be applied to n-MOSFETs.

In an n-well process, substrate serves as common body for all n-MOSFETs. Individual n-wells serve as different bodies for p-MOSFETs. In Chapter 2, forward body-bias can be applied to both of n-MOSFET and p-MOSFET in the amplifier design because all n-MOSFETs have same body-bias voltage. In the adaptive bias design, n-MOSFETs have different body-bias voltage. Thus, we only applied the body-bias to p-MOSFETs. A twin well process is needed to apply different body-biases to both n-MOSFETs and p-MOSFETs.

Figure 5.7 shows the variation of leakage current with the magnitude of threshold voltages in a p-MOSFET of the inverter circuit of Fig. 5.6 with and without reverse body-bias of 0.4 V. The solid line in Fig. 5.7 shows the leakage current with a zero body-bias and the dotted line shows the leakage current with a reverse body-bias of 0.4 V. The leakage current increases with decrease in zero body-biased threshold voltage and is

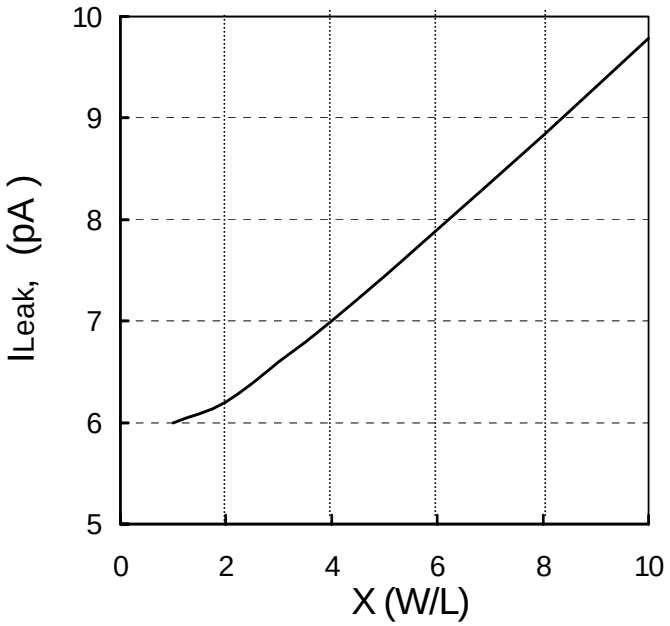

Figure 5.5: SPICE simulated leakage current, I_{leak}, versus X (W/L). W/L is the ratio of a unit size transistor and X is an integral multiplier number. W/L of a unit size n-MOSFET = 2.4/1.6 and p-MOSFET = 4.8/1.6.

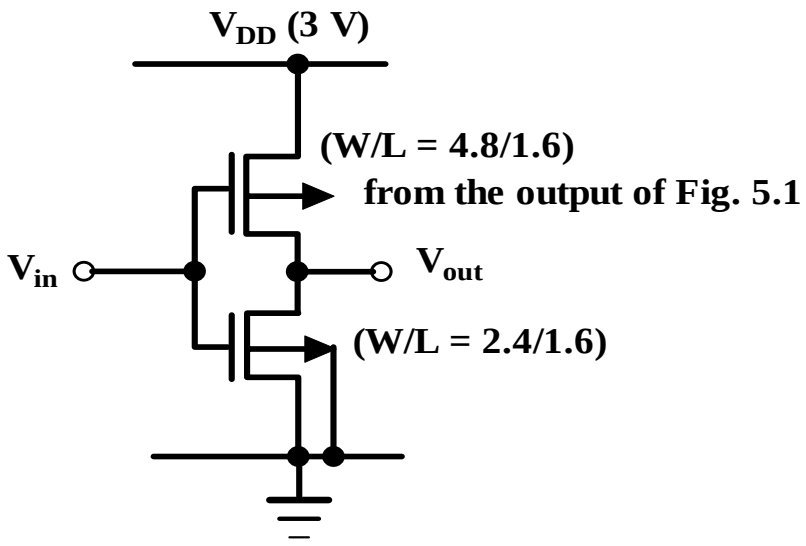

Figure 5.6: A simple inverter to illustrate leakage current reduction.

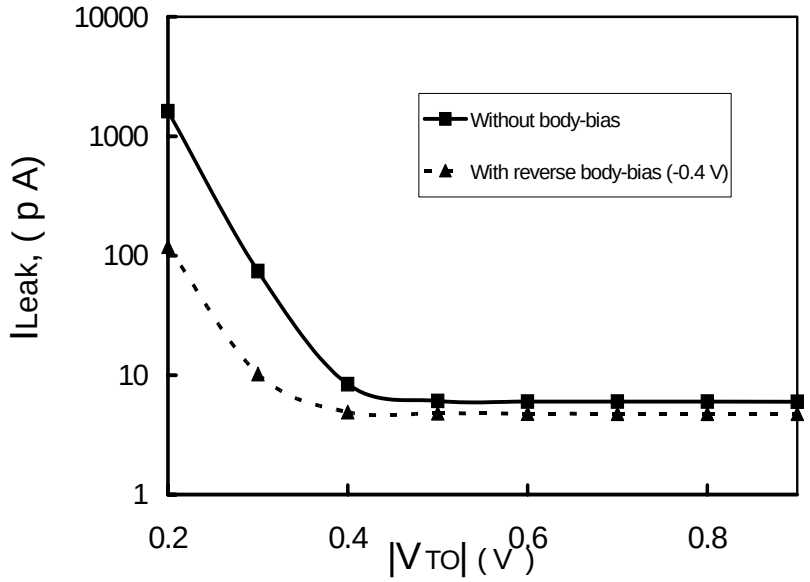

Figure 5.7: SPICE simulated leakage current versus initial zero-biased threshold voltage. Solid line represents leakage current without reverse body-bias. Dotted line represents leakage current with reverse-body bias. $|V_{TO}|$ is a zero-bias threshold voltage.

significant at lower threshold voltages. Notable is the increase in leakage current below the magnitude of 0.4 V without body-bias. Reverse body-bias is very effective in reducing the leakage current for threshold voltages of magnitude below 0.4 V.

Figure 5.8 shows reduction in the static power dissipation in percentage versus the magnitude of threshold voltage. It is seen that up to 92.3% static power dissipation can be saved under off condition when the magnitude of the threshold voltage reduces to 0.2 V.

5.3 Experimental Results

Figure 5.9 shows the layout of an adaptive body-bias generator CMOS circuit. The layout area is 1.5 mm x 1.5 mm. The microphotograph of the fabricated chip in standard 1.5 µm CMOS process is shown in Fig. 5.10. Figure 5.11 shows output waveform of the 3-bit counter and the reference clock. In Fig. 5.11, least significant bit (LSB) of counter is observed. The counter starts counting when the reference clock is low, (“0”) and stops counting when the reference clock goes high, (“1”). In Fig. 5.11, counter counts 4. Table 5.2 shows the truth table of LSB of the 3-bit counter. The 3-bit outputs of counter are then transferred to D-flip flops to select a proper body-bias through the multiplexer.

5. 4 Summary

A frequency adaptive body-bias generator CMOS circuit has been designed, which generates varying body-biases to MOSFETs depending upon the operational frequency. The design is based on frequency comparison of an external reference clock and a pre-designed ring oscillator. Notable reduction in leakage current can be obtained for low threshold MOSFETs. The static power consumption can be saved up to 92.3% in low threshold MOSFET circuits. The adaptive body-bias generator circuit occupies an

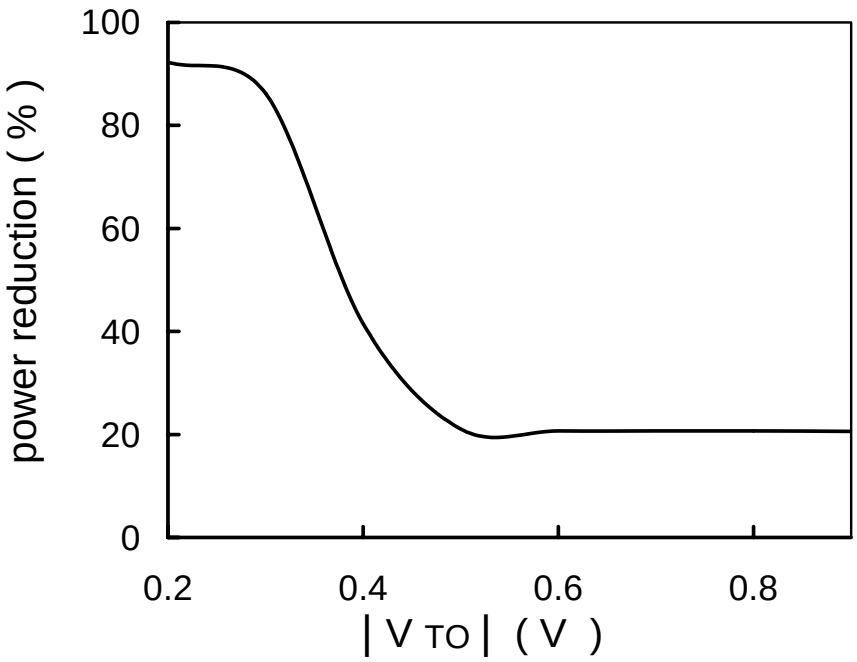

Figure 5.8: Static power reduction versus zero-biased threshold voltage of a CMOS inverter. Power reduction is computed from the reference power dissipation without body-bias applied to the p-MOSFET of the inverter circuit of Fig. 5.6.

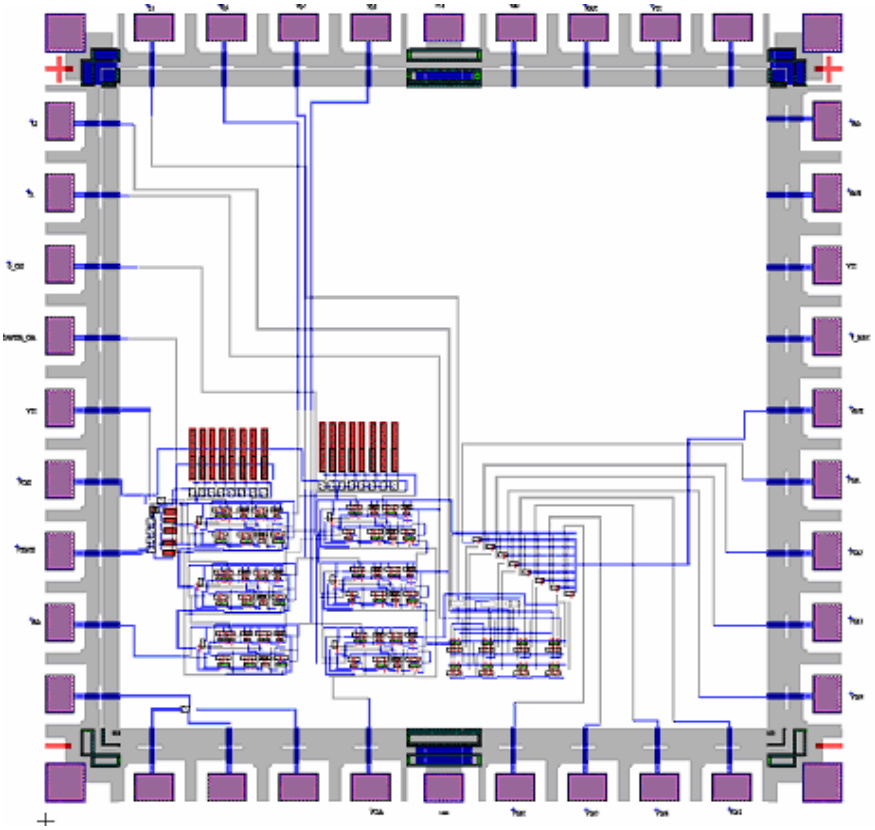

Figure 5.9: Layout of an adaptive body-bias generator CMOS circuit.

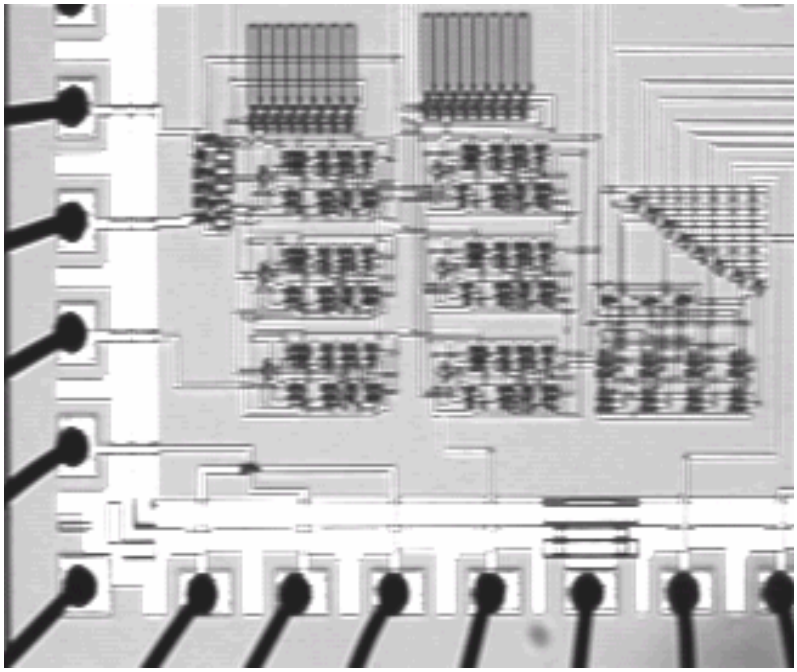

Figure 5.10: Microphotograph of an adaptive body-bias generator CMOS circuit of Fig. 5.9.

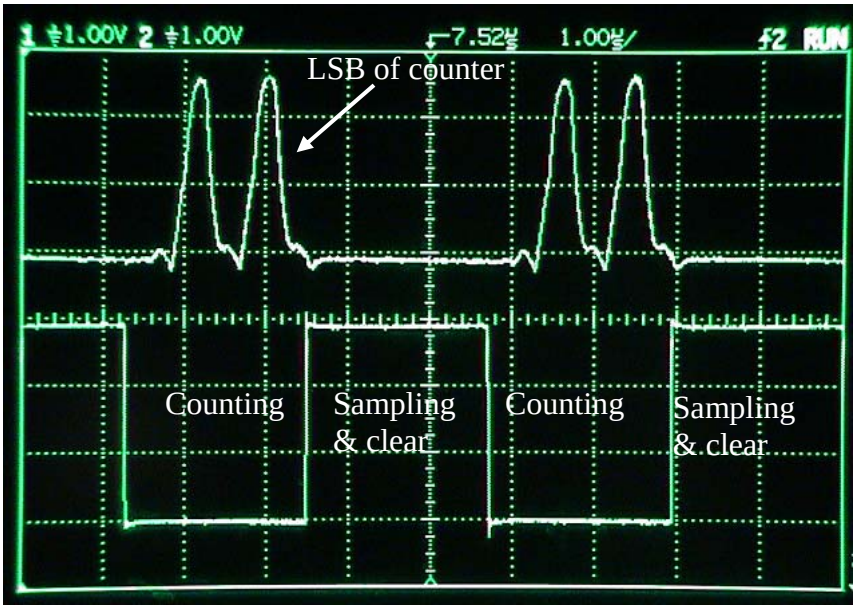

Figure 5.11: Measured waveforms of the least significant bit of the counter and the reference clock. Scale: X-axis: 1µS/div., Y-axis : 1 V/div.

Table 5. 2. Truth table of a 3-bit counter

Most significant bit (MSB)	**Second bit**	**Least significant bit (LSB) (observed in Fig. 5.11)**
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

area of 1.5 mm x 1.5 mm in standard 1.5 µm n-well CMOS process. The design is verified experimentally. The method can lower the leakage current in CMOS chip when the circuit is not operating at its maximum performance. The presented method is simple and can be embedded in a CMOS system design for low voltage operation. In the present design, range of $V_{bias,0}$ to $V_{bias,7}$ is external to 8-to-1 multiplexer part of the circuit of the adaptive body-bias generator.

CHAPTER 6*

ADAPTIVE DC/DC CONVERTER

We mentioned earlier that with the proliferation of battery-operated portable devices such as personal digital assistants (PDAs) and cell phones, low power integrated circuits are highly desirable. Reducing supply voltage to reduce power consumption is widely accepted in low-power IC designs [41-44]. When the system is not in its peak performance, lowering the supply voltage can save significant dynamic power, which shows quadratic dependence on supply voltage, V_{DD}. Another important issue in low power design, which we discuss in this chapter, is dynamic voltage scaling (DVS). In [44], a dynamic voltage scaling method is applied to a processor system to satisfy both the performance and power consumption design targets. When the system is in its high performance, a higher supply voltage is provided. When system is running slow or in standby mode, a lower supply voltage is provided. In such a method, the power saving consumption is significant. An adaptive supply voltage can also be used to compensate processing variations [45] to reduce the leakage currents and improve the reliability.

DC/DC converter is found out to be the best solution in adaptive supply voltage generation [24-27]. Recently, digitally controlled DC/DC converter has drawn wide attention due to its fast response, low power consumption and compatibility with standard digital CMOS processes [25]. Many existing implementations of digital controller need a high-resolution, high-speed analog-to-digital (A/D) converter, which occupies a large chip area and consumes significant power. The A/D converter first samples and then

* Part of this work is reported in the following publication: C. Zhang, D. Ma and A. Srivastava, "Integrated adaptive DC/DC conversion with adaptive pulse-train technique for low-ripple fast response regulation," *Proc. IEEE International Symposium on Low Power Electronics and Design (ISLPED' 04),* pp. 257-262, 2004.

converts the regulated output voltage into digital signals in a feed back loop to determine the duty ratio of the DC/DC converter. Its bandwidth limits the overall dynamic response of the power converter. Delay-line based controllers reported in [26, 27] transform voltage signal into a frequency signal, and use digital signal processing circuits for voltage regulation. Power consumption of delay-line can be much lower than A/D converter implementations [27].

For improved performance and better control, a pulse-train technique is proposed in [28]. By adopting a pulse train instead of a constant pulse as a gate control signal of switches, the converter successfully avoids over charging or discharging of the capacitor during transition. Resolution of the control is thus improved with smaller output ripple voltages. However, the pulse-train technique slows down the transient response since the converter takes a longer time to deliver the energy to the load. In this chapter, an adaptive pulse-train technique is proposed which is incorporated in delay-line controller for low ripple and fast transient response. An internal control signal can enable pulse-train function for high-resolution regulation in a steady mode and disable it for the fast dynamic response in a transient mode.

6.1 DC/DC Converter with Delay-line Based Controller

Delay-line controller is used to replace traditional A/D converter due to its simplicity and low power consumption. However, complex auxiliary logic associated with delay-line may occupy large chip area and increase power consumption. In [26], a look-up table is needed to process an error signal. The look-up is stored in an external memory which is unwanted in integrated design. In [27], a large number of S-R latches and flip flops are used to implement digital control law. In this work, a simple controller

is designed which consists of a delay-line, a few logic gates and adaptive pulse-train technique. Figure 6.1 depicts the block diagram of a delay-line based DC/DC converter. The converter consists of a power stage, a delay-line based digital controller to control the duty ratios of the switches in the power stage and a reference clock.

The delay-line is powered by the output voltage of the converter and is used to detect variations in the output. Its propagation delay, t_d is, thus, inversely proportional to the output voltage, V_{out}. The first order relation is expressed as [46]

$$t_d = \frac{2nKV_{out}}{(V_{out} - V_T)^2} \tag{6.1}$$

where V_T is the threshold voltage of transistors, n presents the number of stages in the delay line and K is a constant parameter related to the fabrication process. The propagation delay increases as V_{out} decreases. A linear relation is observed when V_{out} is much higher than V_T. The resolution of delay line is determined by the number of stages, n. Larger number of stages in the delay-line give more accurate measure on variations of V_{out}. In this work, twenty-stage delay line is employed, which can differentiate a minimum voltage variation of 15 mV at the $V_{out.}$ When the reference clock f_{ref} is applied, it passes through a 20-stage delay line (each delay stage consists of an inverter pair) and is sampled at output of the 20th stage at a fixed sampling rate of $f_{ref.}$ The propagation delay, t_d is determined by its supply voltage, V_{out}. When V_{out} decreases, t_d of the delay line increases accordingly. Thus, after a time period of 1/ f_{ref}, the falling edge of the clock signal does not reach the 20th delay stage, as shown in Fig. 6.2(a). The output of the 20th stages keeps its initial value, "1", to charge the capacitor in power stage and increase the

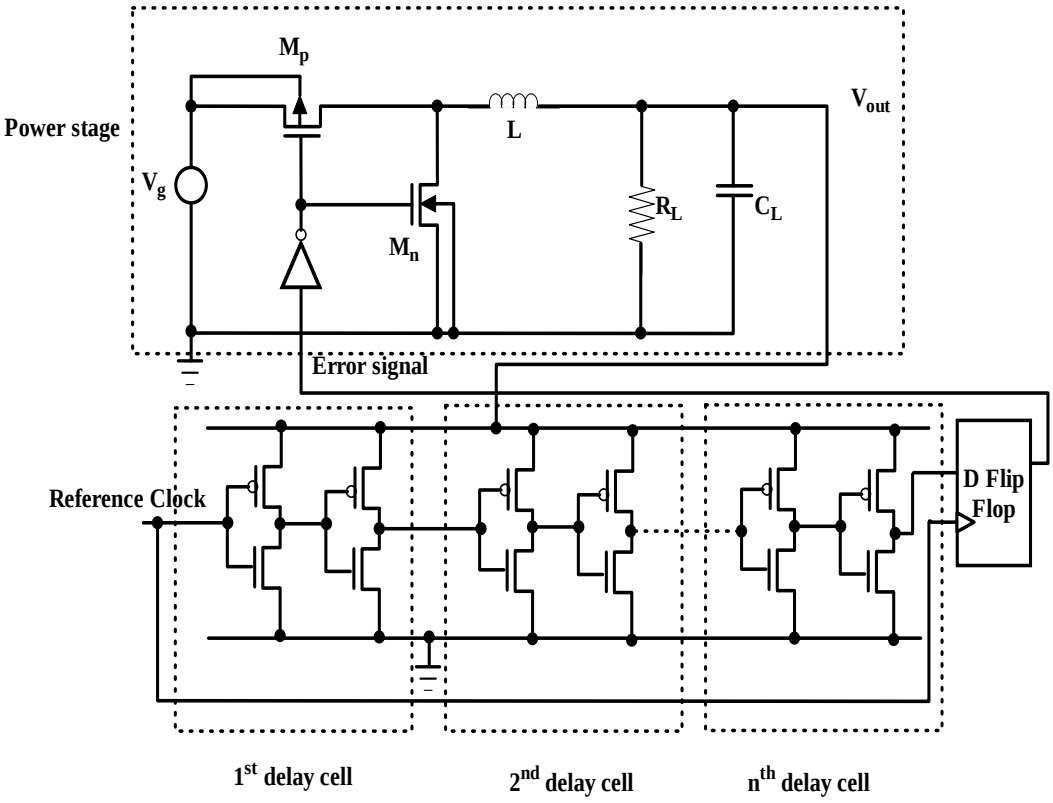

Figure 6.1: Schematic of a delay-line based DC/DC converter.

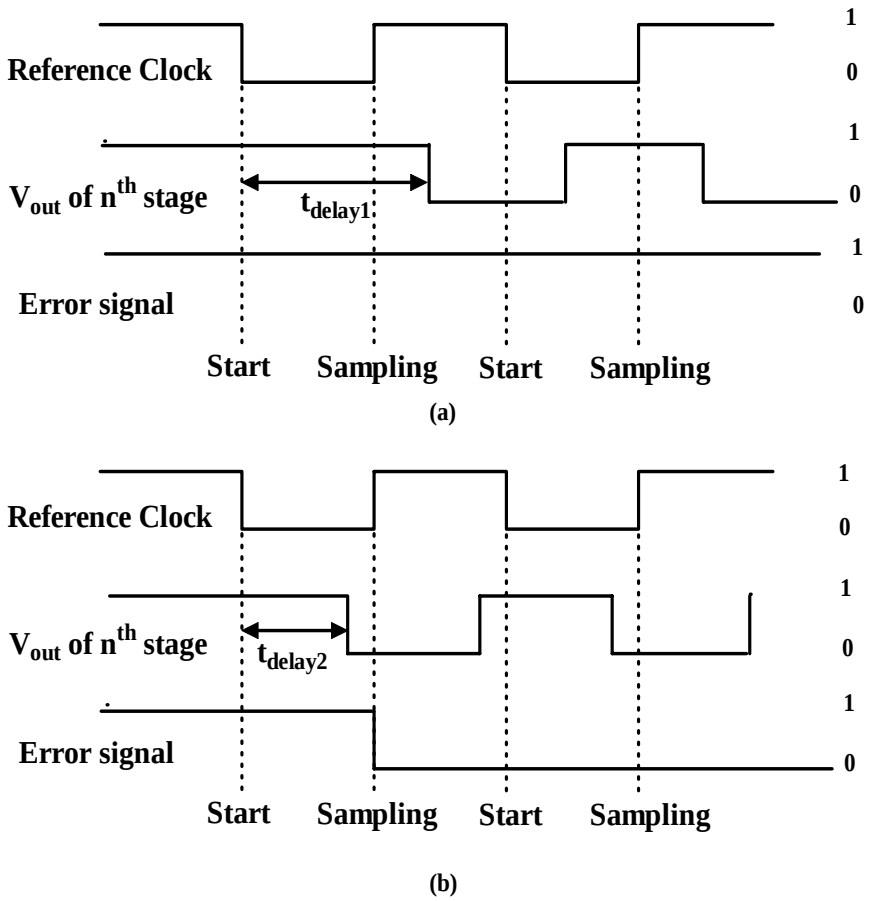

Figure 6.2: Timing diagrams of the converter (a) when V_{out} is too low and (b) when V_{out} is too high.

supply voltage. On the other hand, when V_{out} increases, t_d of the delay line decreases. Thus, after time of $1/f_{ref}$, the falling edge of reference clock has passed the 20^{th} delay stage as shown in Fig. 6.2(b). The output of the 20^{th} stages becomes "0", to discharge capacitor in the power stage and decreases the supply voltage. Thus, the output voltage will be regulated at the desired level with small ripple voltages.

On the other hand, the converter can also be regulated by a variable reference clock signal. Figure 6.3 shows the timing diagram of a DC/DC converter in this case. The higher frequency is associated with a longer duty ratio of the converter, while the low frequency is associated with a shorter one. So the DC/DC converter is frequency-adaptive. The duty ratio is given by the ratio of V_{out}/V_g. V_g is supply voltage. Figure 6.4 shows the relation of V_{out} to the reference clock frequency.

During operation of DC/DC converter, the current in inductor always flows from power supply side to load side. Thus no current flows back to ground through n-MOSFET during discharge phase, thereby giving maximum power transfer efficiency. Figure 6.5 shows simulated results of inductor current.

6.2 Proposed Adaptive Pulse-train Technique

The original pulse-train technique was proposed in [27]. Its concept is illustrated in Fig. 6.6. Now, the duty ratio error signal of the converter is modulated by a pulse train through an AND gate. As a result, the pulse train signals charge and discharge the inductor in the power stage in finer steps. The charging procedure is completed by a few pulses instead of one single period. It reduces the high-peak inductor current and overcharging, thus lowers the ripples at the output voltage, V_{out}. In addition, complexity of design remains almost unchanged since only a few logic gates are added. However,

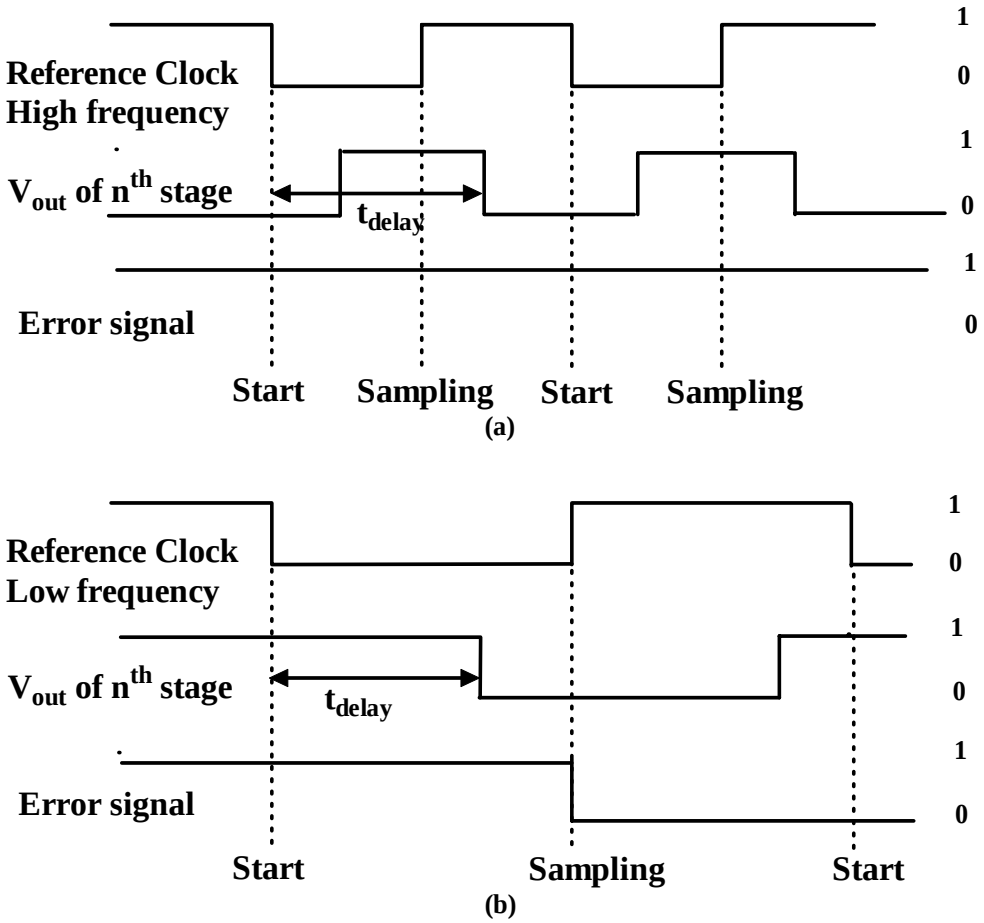

Figure 6.3: Timing diagram of the converter (a) when reference clock frequency increases and (b) when reference clock frequency decreases.

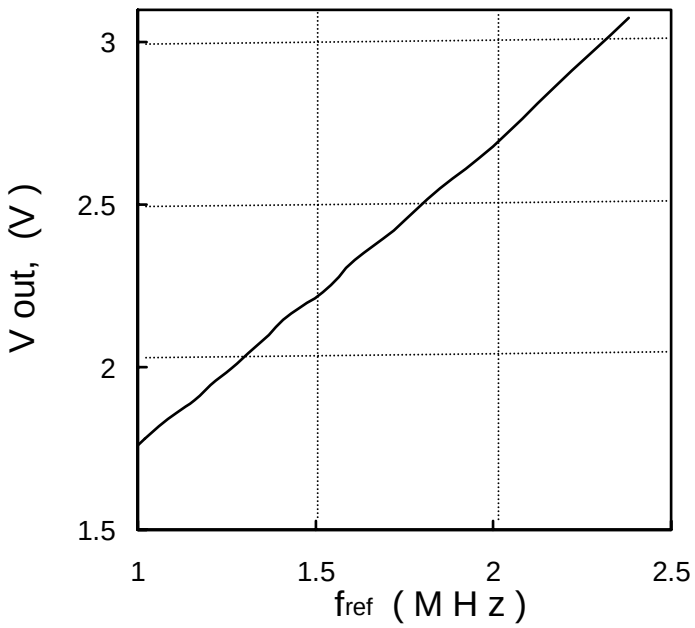

Figure 6.4: Adaptive output voltage, Vout versus the reference clock frequency, f_{ref}.

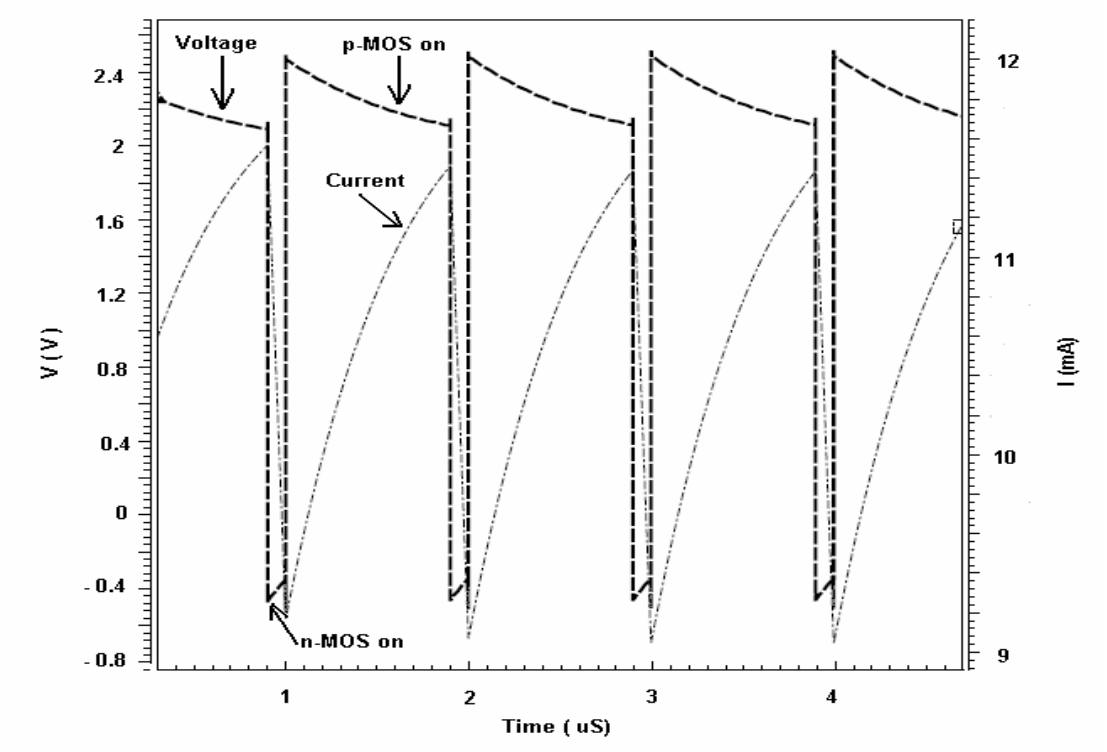

Figure 6.5: Simulated results of current flow in the inductor and voltage on the left side of the inductor shown in Fig. 6.1.

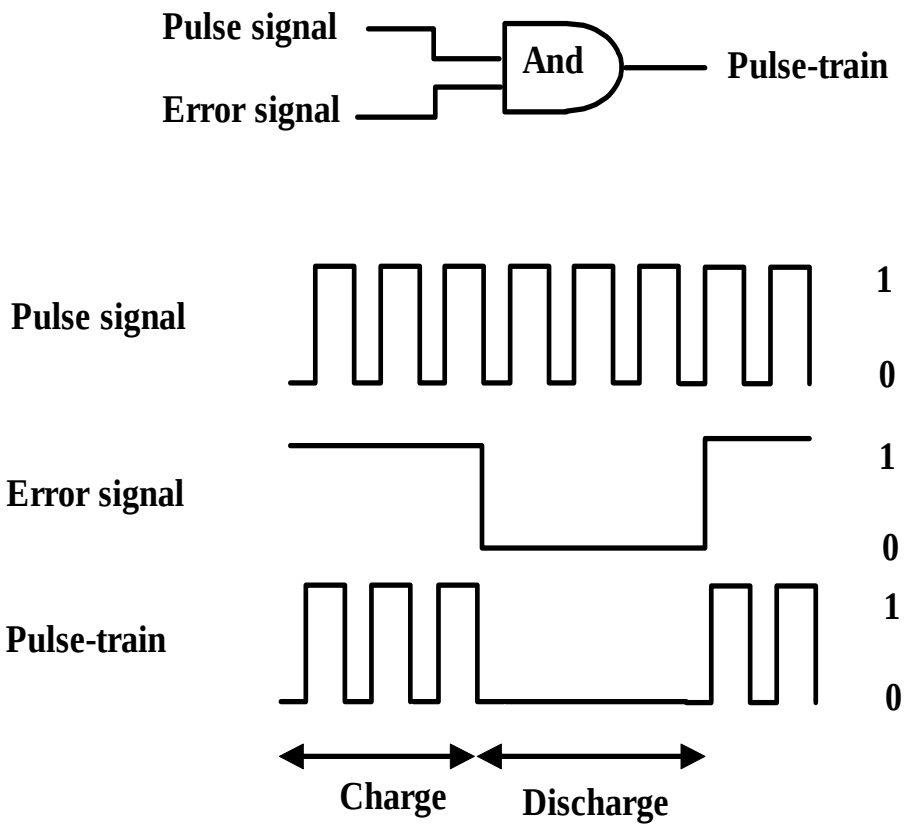

Figure 6.6: Illustration of pulse-train error signal.

this pulse-train technique extends the transient response time (from 50 μS to 100 μS) as shown in Fig. 6.7 since a longer charging period is required to deliver enough current to the load, which greatly degrades the dynamic performance of the adaptive converter. An adaptive pulse-train technique is thus proposed for the fast transience. The circuit diagram is shown in Fig. 6.8.

The technique presented in Fig. 6.8 allows the converter to operate in two different operation modes: transient mode for fast response and steady mode for small ripple voltage. Three XORs are used to detect the falling edge of the reference clock. If the falling edge is detected at the outputs of 19^{th}, 20^{th} or 21^{st}, it means that the output is very close to its destined value and the output voltage is at the quasi-steady mode. In the quasi-steady mode, the pulse-train is enabled to give slow charging and small ripple. If the falling edge is out of detectable range, it means that it is in the transient mode. In a transient mode, the pulse-train is disabled and controller could give large charging current to enhanced the transient response. Figure 6.9 shows the post-layout simulations of transient response with traditional pulse-train technique and the proposed adaptive pulse-train technique. It is seen that the adaptive pulse-train reduced the transient time by 50 % and kept the output ripple low.

The duty ratio of pulse is generated by the circuitry in Fig. 6.10. The output voltage is compared with an external ramp signal. Duty ratio is determined by the trip point. Higher output voltage gives the high duty ratio. The amplitude of ramp, V_{ramp}, is set slightly lower than V_g (V_{ramp} = 3 V in the design) so that the duty ratio is high enough to charge up the output voltage. Figure 6.11 shows that the output ripple voltage decreases as the number of pulses increases in the charging phase when M_p in Fig. 6.1 is

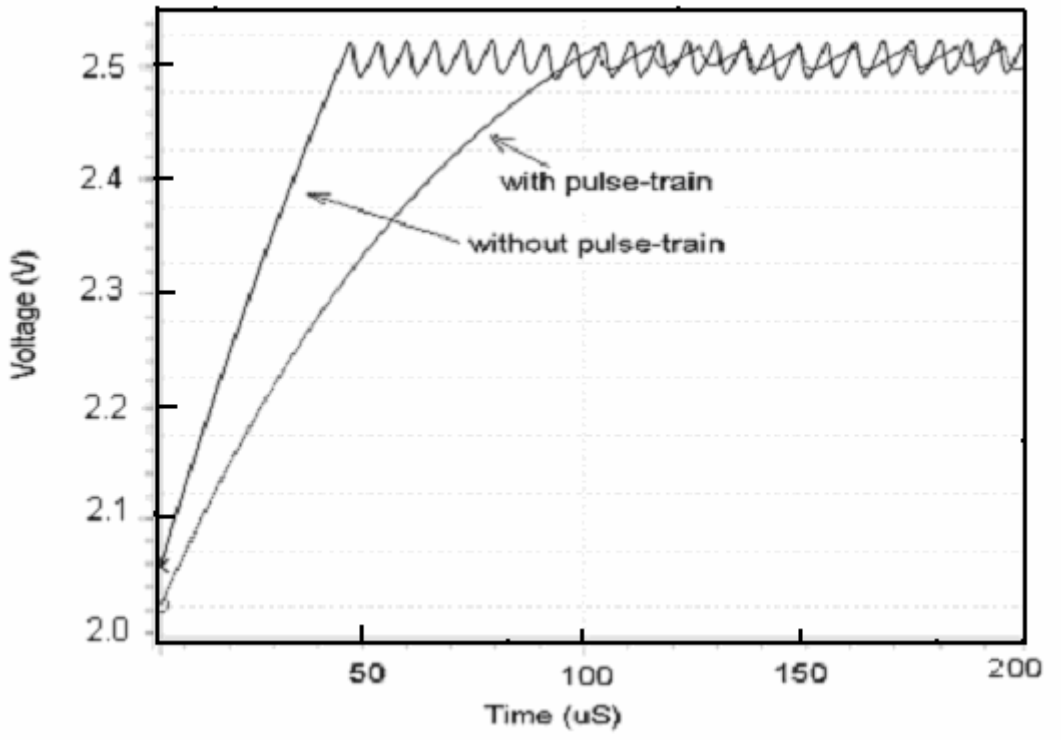

Figure 6.7: Transient response of a converter with and without pulse-train technique.

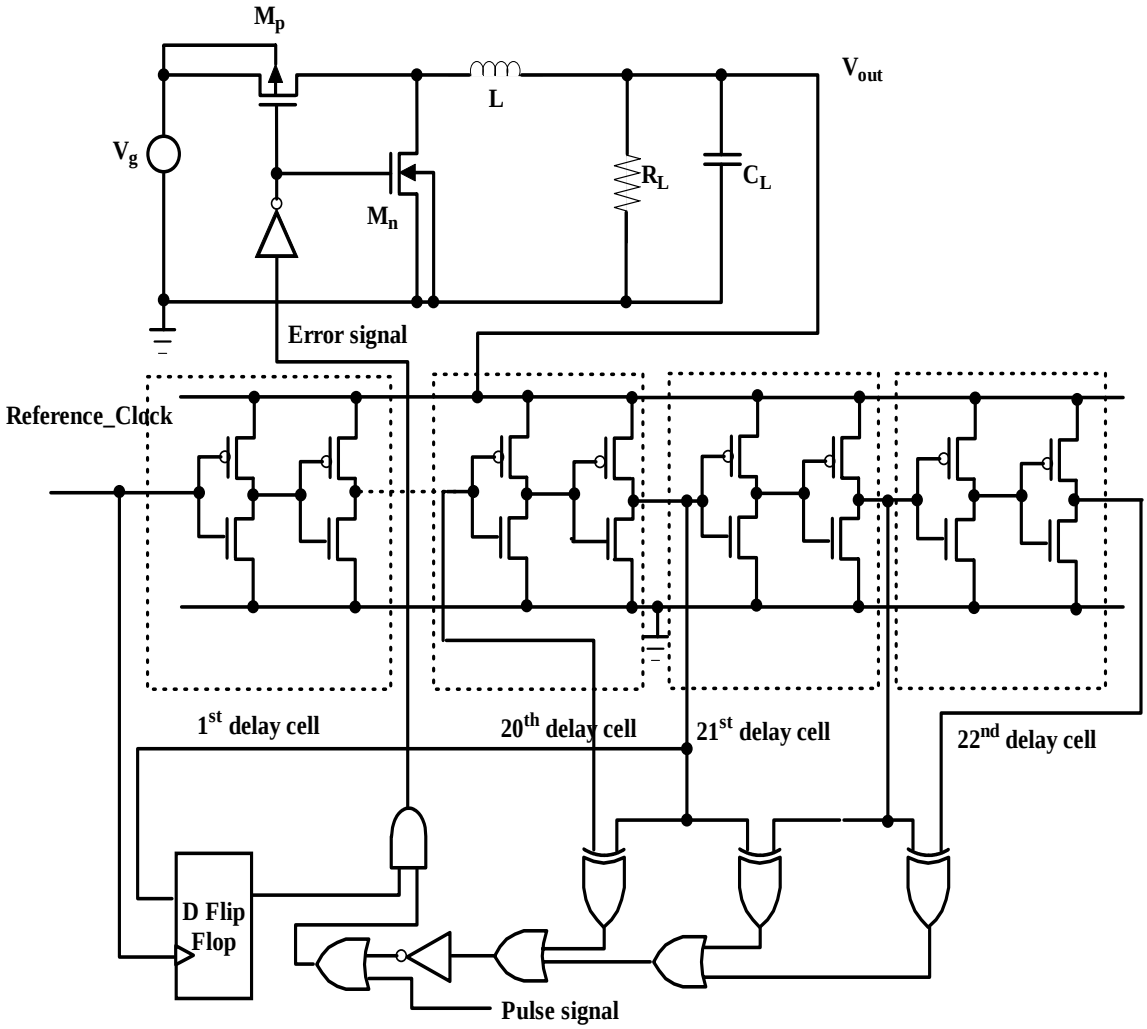

Figure 6.8: Circuit diagram of a DC/DC converter using an adaptive pulse-train technique.

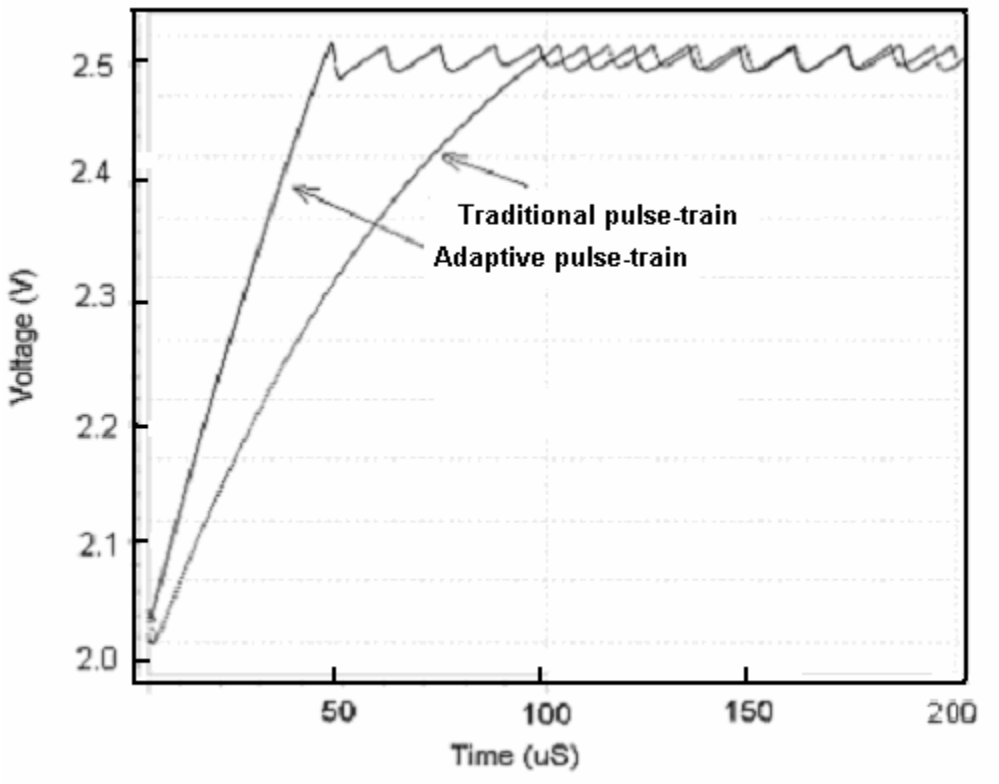

Figure 6.9: Transient response of the output voltage using an adaptive pulse-train technique.

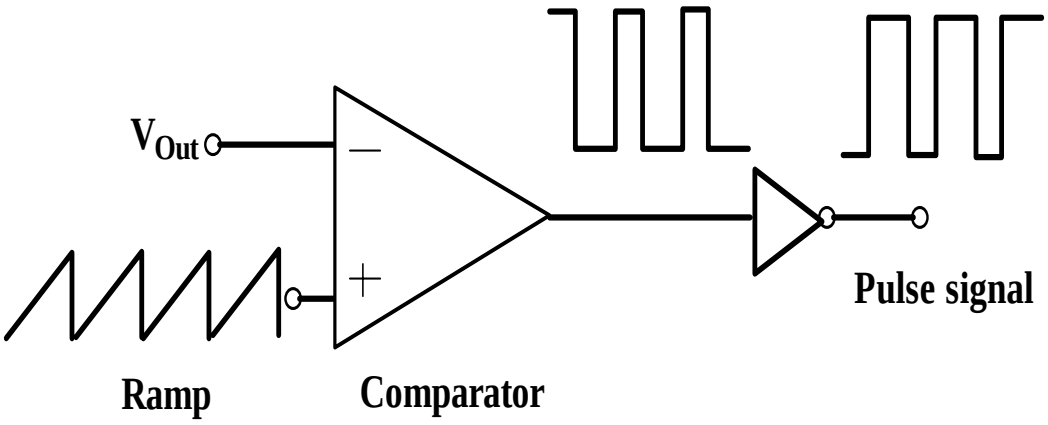

Figure 6.10: Block diagram of a pulse width modulation circuit.

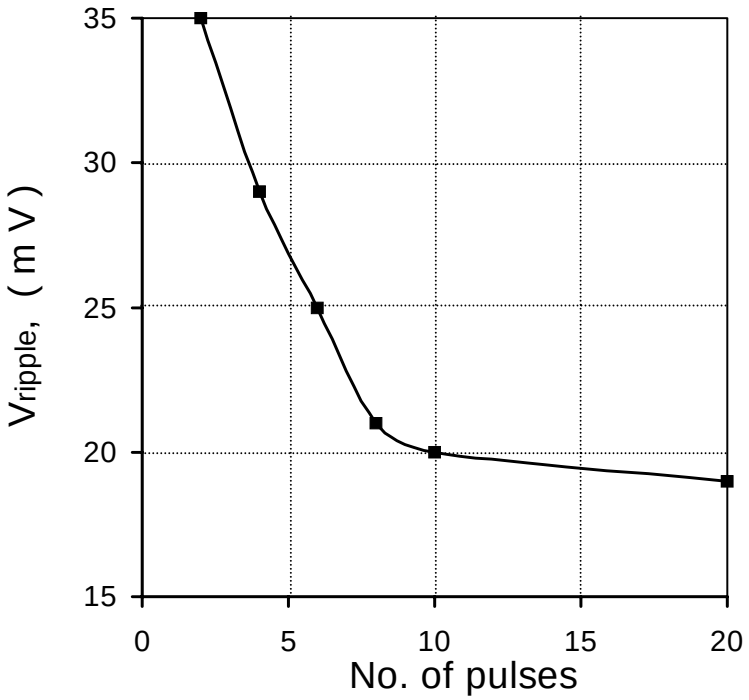

Figure 6.11: Ripple voltage versus number of pulses in one switching cycle.

turned on. A pulse frequency of 2 MHz is selected which ensures 10 pulses in a single charging phase. Figure 6.12 shows the regulated output voltage with a pulse frequency of 2 MHz. The frequency of reference clock is 1.8 MHz. Figure 6.12 shows that the pulse-train technique reduces ripple by 50%, thus giving output voltage ripple of 18 mV. The reduction of ripple is due to low charging current which is shown in Fig. 6.13.

The current in the inductor charges and discharges the load capacitor. The capacitor does not dissipate energy, therefore the average current is zero. Variation of charges in the capacitor causes the output voltage ripple. Ripple in the delay-line controller DC/DC converter is given by [29]

$$V_{ripple} = \frac{I'_{\max} T'}{2C_L} + \frac{I'_{\max} t_{loop}}{C_L}. \tag{6.2}$$

In Eq. (6.2), I'_{max} is the ideal maximum charging current in the capacitor without considering delay of feedback loop. T' is the ideal charging time and t_{loop} is the delay of the feedback loop and is equal to $T_1 - T_1'$. Here T_1 is the actual charging time. The first term in Eq. (6.2) is the system ripple determined by resolution of the delay-line controller. The second term in Eq. (6.2) is determined by maximum charging current. The maximum charging current without pulse-train technique is expressed as [29]

$$I'_{\max 1} \approx I_{\max 1} = T_1 \frac{V_g - V_{out}}{L} \tag{6.3}$$

where L is the inductance. The maximum charging current with the pulse-train technique is given by [29]

$$I_{\max 2} = T_2 \left[\frac{V_g - V_{out}}{L} D - \frac{V_{out}}{L}(1 - D) \right] \tag{6.4}$$

where D is the duty ratio of the pulse. Further simplifying Eq. (6.4), we obtain

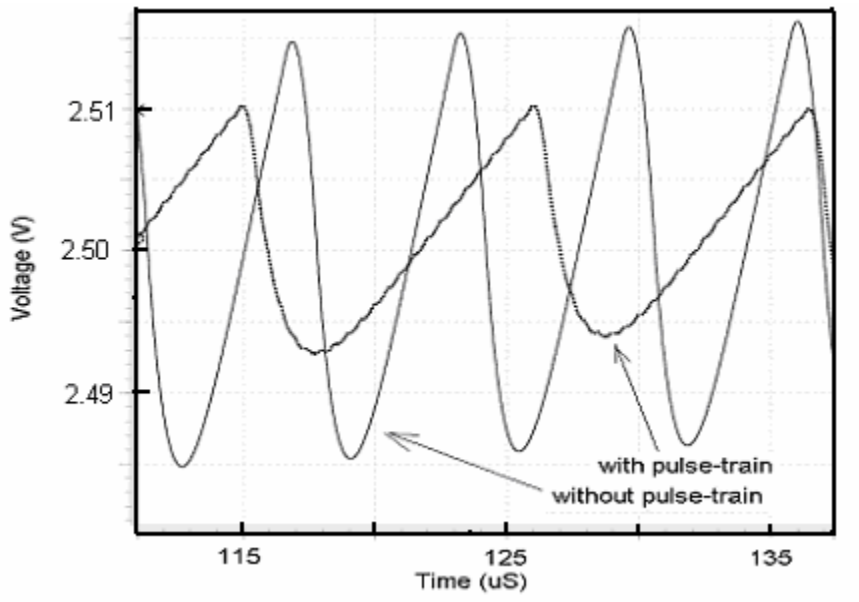

Figure 6.12: Output voltage ripple with and without pulse-train technique.

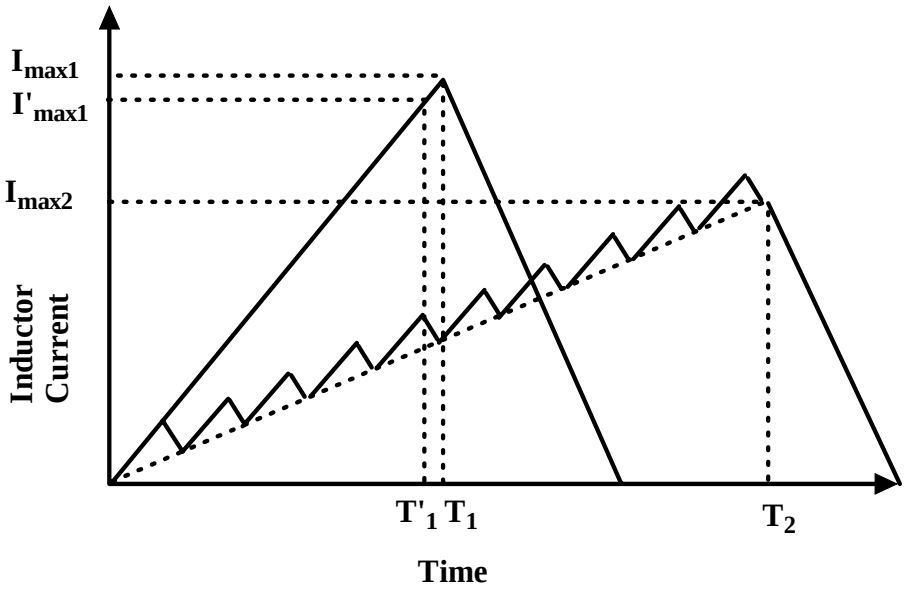

Figure 6.13: Inductor current of the converter with and without pulse-train technique in steady state (only the charging phase is shown).

$$I_{\max 2} = \frac{T_2 V_{out}}{L}\left(\frac{V_g}{V_{out}} D - 1\right) \tag{6.5}$$

where T_2 is the charging time in a single charging phase with the pulse-train technique. In Eq. (6.5), if D = 1, the pulse-train technique does not apply. If $D = V_{out}/V_g$, then the maximum current will be zero. The duty ratio is set to about 10% higher than V_{out}/V_g as generated by the circuit of Fig. 6.10. The duty ratio ensures a low maximum charging current.

In real situations, there is always an equivalent series resistance (ESR) connected with the output capacitor, C_L. It exaggerates ripples of the output voltage as shown in Fig. 6.13. With an adaptive pulse-train technique, low ripples are still obtained. The shapes in the output voltage of Fig. 6.14 using adaptive pulse-train control reflect finer charging steps in a single charging phase. The ripple is reduced to 22 mV from 36 mV. Benefiting from low power consumption of the digital controller, maximum efficiency of 92 % is achieved for power transfer to load when the converter is regulated at 2.5 V with an output power of 125 mW. The inductor (L) and capacitor (C_L) of DC-DC converter are 4.7 µH and 10 µF, respectively.

Results presented are obtained from the post-layout simulations. The layout area is 0.8 mm x 1.2 mm using 1.5 µm standard two-metal, two-poly, digital CMOS process and is shown in Fig. 6.15. Design in [26] without external memory occupies 1 mm x 1 mm silicon area in 0.5 µm CMOS technology. Design in [25] takes 1.1 mm x 1.3 mm area in 0.25 µm CMOS technology. Compared with [25] and [26], the present design uses less area on a chip.

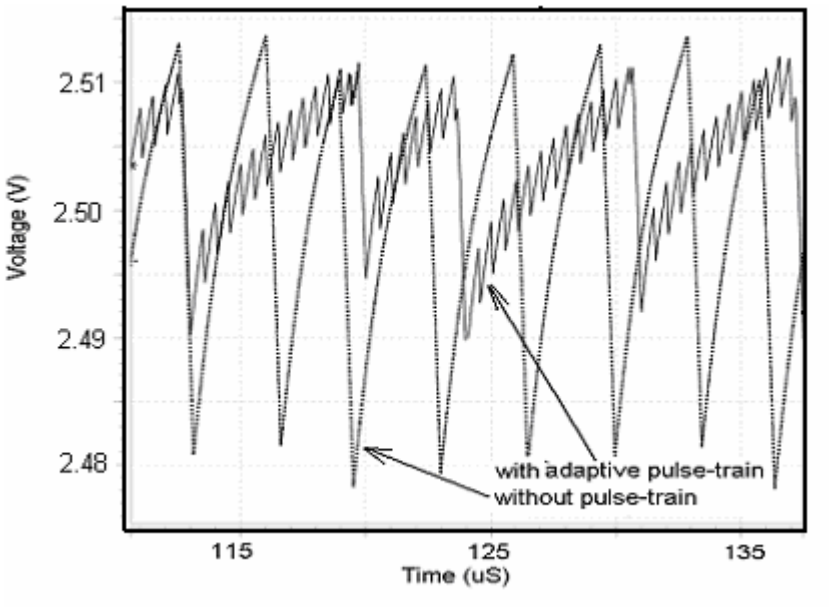

Figure 6.14: Ripple of the output voltage with ESR.

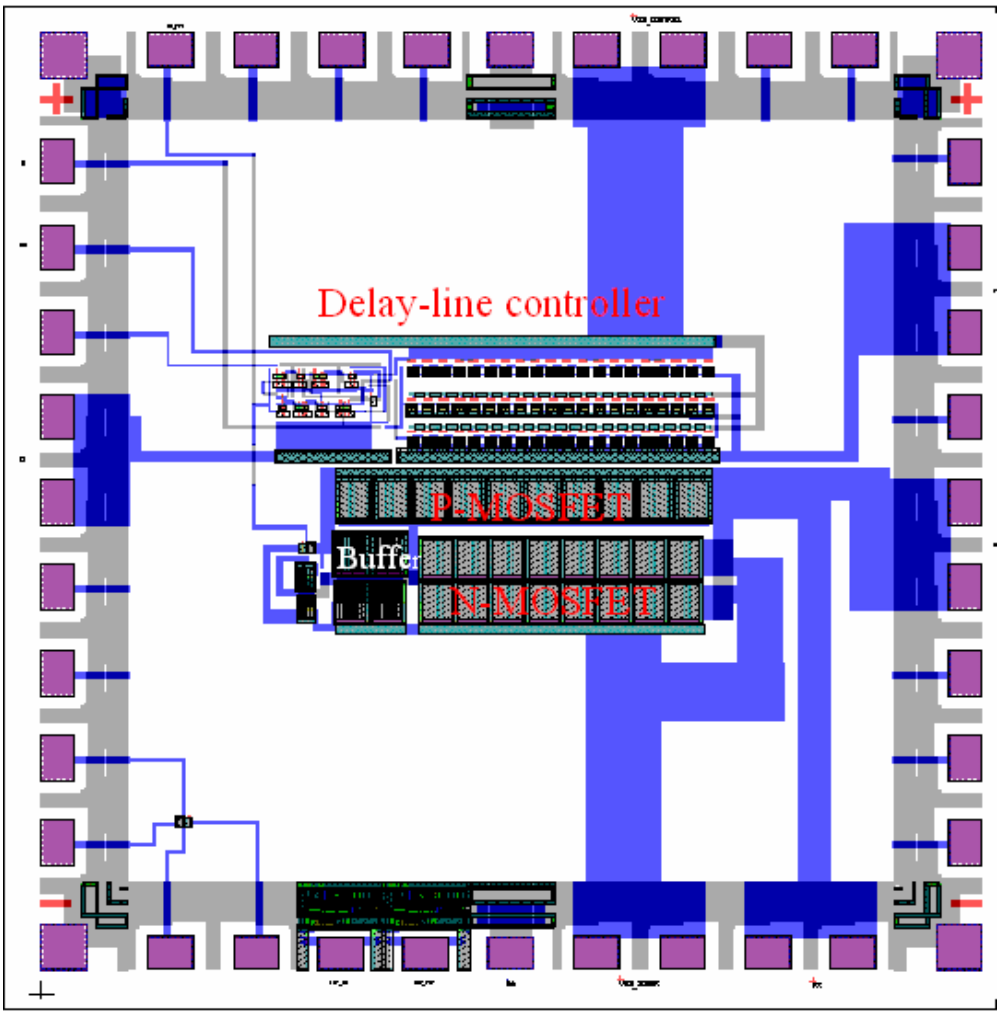

Figure 6.15: Layout of an adaptive DC/DC converter using the delay-line based controller and an adaptive pulse-train technique.

6.3. Summary

An adaptive high power efficiency DC/DC converter is designed which is based on a low power delay-line controller and an adaptive pulse-train technique. The power consumption of controller is less than 100 μW, which is much lower than the traditional controller. Maximum power efficiency of 92 % is obtained with an output power of 125 mW. The controller operates in two modes: transient mode and quasi-steady mode. Adaptive pulse-train technique enables the pulse-train technique in steady mode for the low current charging thereby reducing the output ripple voltage. The output ripple is reduced by 50 %. The pulse-train is disabled in transient mode keeping high transient response. Compared with the traditional pulse-train technique, response time is reduced by 50 % in the transient mode where high transient speed is highly desirable. An equivalent series resistor, 100 mΩ is also added for the post layout simulation. The adaptive pulse-train technique keeps its ripple below 22 mV. With a supply voltage V_g of 3.3 V, the output is regulated over the range of 1.7 to 3.0 V.

CHAPTER 7

CONCLUSION AND SCOPE FOR FUTURE WORK

In this work, several low power techniques for the design of CMOS integrated circuits design are proposed, which are summarized as follows.

7.1 Forward Body-Bias Technique and CMOS Amplifier

Threshold voltage of a MOSFET can be reduced electrically by forward biasing the source-substrate (body) junction which helps in reducing the supply voltage. The power dissipation which is proportional to the square of the supply voltage, is thus reduced. Based on this forward body-bias technique, an amplifier has been designed for operation at 0.8 V (± 0.4V) in 1.5 μm n-well CMOS process. The forward body-bias is limited to 0.4 V due to CMOS latchup. The measured gain is nearly 58 dB with a 3 dB 30 kHz bandwidth. The power consumption close to 80 μW is extremely small. The low power CMOS amplifier can be used in portable, biomedical devices and microsystems.

7.2 Noise in the Forward Body-Bias MOSFET

Noise introduced by forward body-bias in a MOSFET is analyzed. Both the simulation and the analytical model show that the thermal noise decreases and shot noise increases with the increasing forward bias between the source and substrate junction in a MOSFET. The shot noise increases exponentially with increasing the forward body-bias. The shot noise becomes significant over the thermal noise for the forward body-bias above 0.4 V. The flicker noise (1/f noise) is not considered because the low drain current and forward body-bias conditions in a MOSFET suppress it. Ultra low-power amplifier is designed using the forward body-biased technique for operation at 0.8 V (± 0.4 V). The output noise of ultra low-power amplifier is 360 x 10^{-12} V^2/Hz. It is shown that the 0.4 V

forward body-bias technique combined with the low voltage operation does not introduce significant noise in CMOS ultra-low power amplifier and does not trigger the latchup action. The simulated input noise spectral density of the forward body-biased CMOS operational amplifier is in close agreement with the corresponding value of TI OPA349 CMOS operational amplifier.

7.3 Dynamic Threshold MOSFET Technique and Novel Schmitt Trigger Circuits

Two circuits are designed using the dynamic body-bias technique. A 0.8 V low voltage analog multiplexer is designed. It can be integrated on a chip with sensors to preprocess low voltage signals such as biological or chemical signals with reduced noise and distortion. The dynamic body-bias technique is applied to a sub-circuit design such as switch and inverter to reduce signal leakage while maintaining low voltage operation. An improved dynamic threshold MOSFET (DTMOS) configuration ensures the forward body bias below 0.4 V.

Novel low voltage CMOS Schmitt trigger circuits have been implemented in standard 1.5 μm CMOS process for operation at 1 V and 0.4 V using the DTMOS technique. This method exploits lowering of the threshold voltage of a MOSFET under the forward body-bias. Measured hysterisis widths agree closely with the corresponding calculated value of 0.15 V. The proposed CMOS Schmitt trigger circuit is extremely useful in low/ultra-low voltage circuit applications where waveform shaping is needed under noisy conditions.

7.4 Adaptive Body-Bias Generator

A frequency adaptive body-bias generator CMOS circuit has been designed, which generates varying body-biases to MOSFETs depending upon the operational

frequency. The design is based on frequency comparison of external reference clock and the pre-designed ring oscillator. Notable reduction in leakage current can be obtained for low threshold MOSFETs. The static power consumption can be saved up to 92.3% in low threshold MOSFET circuits. The adaptive body-bias generator circuit occupies an area of 1.5 mm x 1.5 mm in standard 1.5 μm n-well CMOS process. The design is verified experimentally. The method can lower leakage current in CMOS chip when the circuit is not operating in its maximum performance. The presented method is simple and can be embedded in a CMOS system design for low voltage operation. In the present design, range of $V_{bias,0}$ to $V_{bias,7}$ is external to 8-to-1 multiplexer part of the circuit of the adaptive body-bias generator. The on-chip adaptive body-bias generator is suggested for the future work.

7.5 Dynamic Voltage Scaling and DC/DC Converter

An adaptive high efficiency DC/DC converter is designed which is based on a low power delay-line controller and an adaptive pulse-train technique. The power consumption of controller is less than 100 μW, which is much lower than the traditional controller. Maximum power efficiency of 92 % is obtained with an output power of 125 mW. The controller operates in two modes: transient mode and quasi-steady mode. The adaptive pulse-train technique enables the pulse-train technique in a steady mode for the low current charging thus reduces the output ripple voltage. The output ripple is reduced by 50 %. The pulse-train is disabled in transient mode keeping high transient response. Compared with traditional pulse-train technique, response time is reduced by 50 % in transient mode where high transient speed is highly desirable. An equivalent series resistor, 100 mΩ, is also added for post layout simulation. The adaptive pulse-train

technique keeps ripple below 22 mV. With a supply voltage V_g of 3.3 V, the output is regulated over a range of 1.7 to 3.0 V.

7.6 Scope for Future Work

The forward body-bias amplifier and the dynamic body-bias switches could be used in mixed-signal CMOS circuit modules such as the analog-to-digital converter and the digital-to-analog converter. The adaptive body-bias generator can be used to suppress the leakage current in I_{DDQ} testing of sub-micron/deep sub-micron CMOS integrated circuits. Leakage current is one of the important issues in current CMOS technique. The adaptive DC/DC converter can be used to power up microprocessors and also to power up multi-core microprocessors. The low voltage design techniques can be easily applied to designs of ultra-low power analog, digital and mixed-signal circuits in deep sub-micron CMOS process.

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APPENDIX A

MOSIS SPICE LEVEL 3 MOS MODEL PARAMETERS FOR A STANDARD N-WELL CMOS TECHNOLOGY

The following SPICE level 3 MOS model parameters used in simulation have been obtained from the following website: www.mosis.org.

(A) Model Parameters for n-MOS transistors.

```
.MODEL NMOS NMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U
+ TPG=1 VTO=0.587 DELTA=0.0000E+00 LD=1.0250E-07 KP=7.5564E-05
+ UO=671.8 THETA=9.0430E-02 RSH=2.5430E+01 GAMMA=0.7822
+ NSUB=2.3320E+16 NFS=5.9080E+11 VMAX=2.0730E+05 ETA=1.1260E-01
+ KAPPA=3.1050E-01 CGDO=1.7294E-10 CGSO=1.7294E-10
+ CGBO=5.1118E-10 CJ=2.8188E-04 MJ=5.2633E-01 CJSW=1.4770E-10
+ MJSW=1.00000E-01 PB=9.9000E-01
```

(B) Model Parameters for p-MOS transistors.

```
.MODEL PMOS PMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U
+ TPG=-1 VTO=-0.7574 DELTA=2.9770E+00 LD=1.0540E-08 KP=2.1562E-05
+ UO=191.7 THETA=1.2020E-01 RSH=3.5220E+00 GAMMA=0.4099
+ NSUB=6.4040E+15 NFS=5.9090E+11 VMAX=1.6200E+05 ETA=1.4820E-01
+ KAPPA=1.0000E+01 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=4.2580E-10 CJ=2.9596E-04 MJ=4.2988E-01 CJSW=1.8679E-10
+ MJSW=1.5252E-01 PB=7.3574E-01
```

APPENDIX B

MOSFET MODELING

The key MOSFET model parameters can be extracted from the experimental measured current-voltage. The drain characteristics current in saturation region is described by

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2, \qquad (V_{GS} - V_T) < V_{DS} \tag{B.1}$$

where I_D is the drain current and μ is the surface mobility. C_{ox} is gate oxide capacitance per unit area. W/L is channel width to channel length ratio. V_{GS} and V_{DS} are the gate to source voltage and drain to source voltage, respectively. V_T is the threshold voltage.

The Eq. (B.1) cab be rewritten as

$$\sqrt{I_D} = \{\frac{\mu C_{ox}}{2}\frac{W}{L}\}^{\frac{1}{2}}(V_{GS} - V_T). \tag{B.2}$$

The measured $\sqrt{I_D}$ versus V_{GS} of a p-MOSFET is plotted in Fig. B.1. for varying body-biases. The p-MOSFET is operated at V_{DS} equal to 1 V which ensures the saturation region of operation. The tangent to the curve intercepts the X-axis, which gives the threshold voltage, V_T and the slope gives $\sqrt{\frac{\mu C_{OX}}{2}\frac{W}{L}}$. The process transconductance parameters, $\frac{\mu C_{ox}}{2}$ is obtained from the slope and is $13.8\frac{\mu A}{V^2}$. The measured $\sqrt{I_D}$ versus V_{GS} of an n-MOSFET with varying body-biases is plotted in Fig. B.2. The process transconductance parameters, $\frac{\mu C_{ox}}{2}$ from the Fig. B.2. is $34.7\frac{\mu A}{V^2}$. The threshold voltages which are extracted from Fig. B.1 and B.2 are plotted in Fig. B.3.

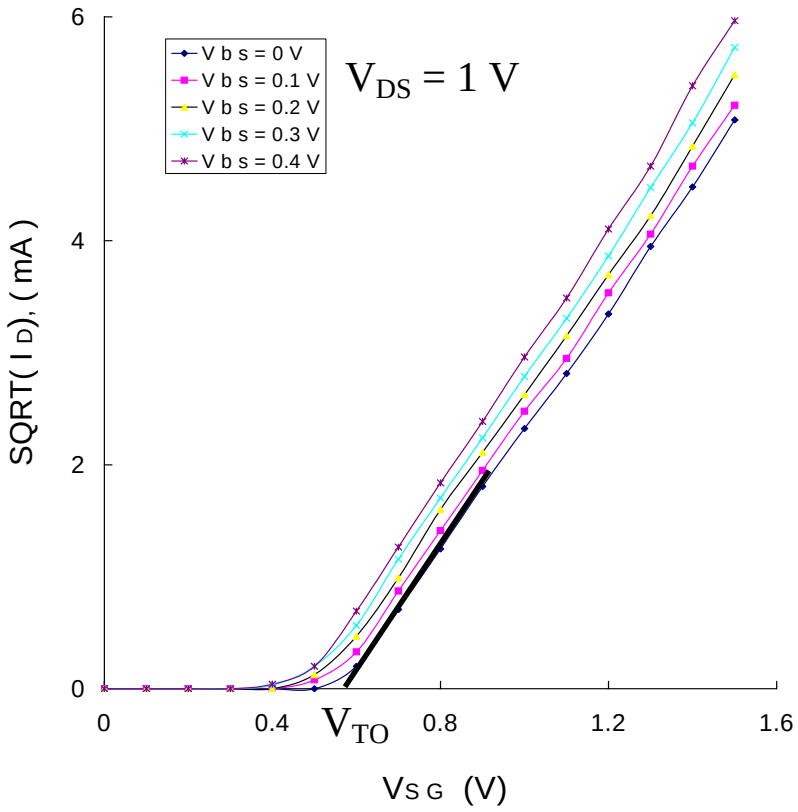

Figure B.1: The plot of $\sqrt{I_D}$ versus V_{GS} of a p-MOSFET (W/L = 6/2).

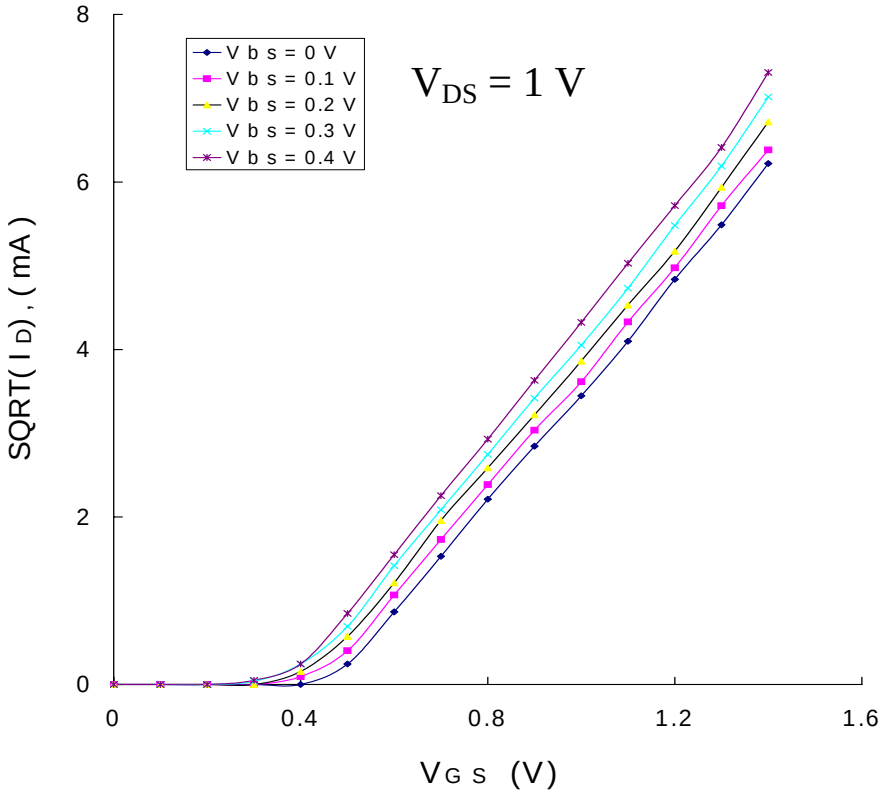

Figure B.2: The plot of $\sqrt{I_D}$ versus V_{GS} of an n-MOSFET (3/2).

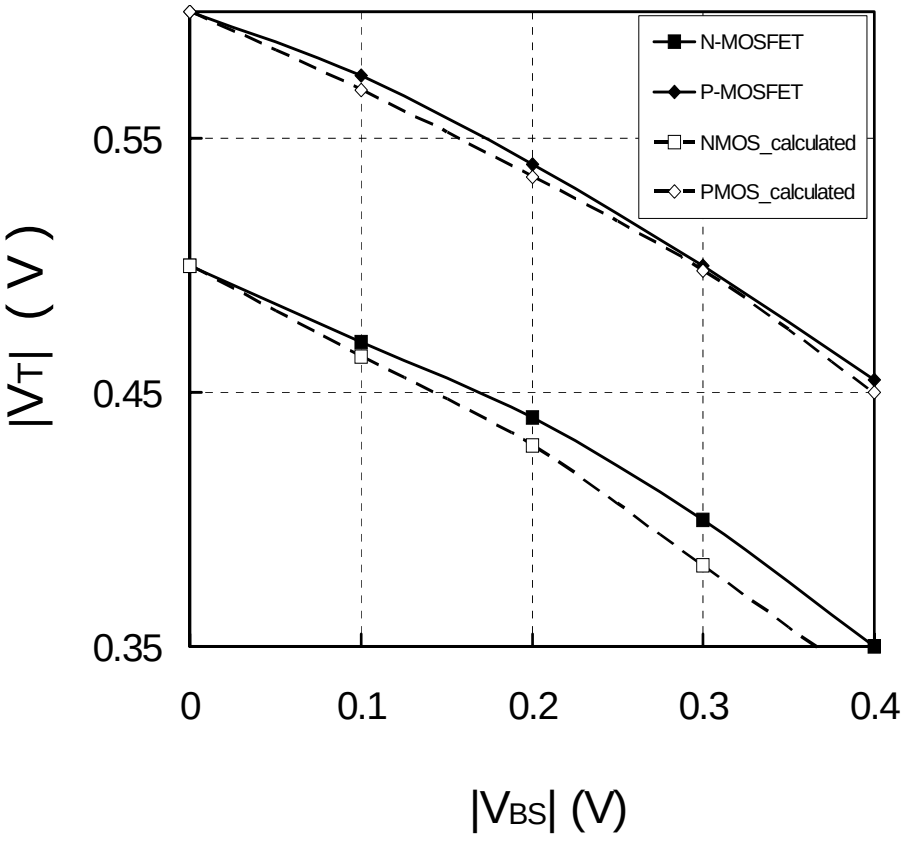

Figure B.3: Magnitude threshold voltage of p- and n-MOSFETs versus the forward body-bias voltage.

Figure B.4 and B.5 show the variation of threshold voltage, V_T with $(\sqrt{|\phi_o|} - \sqrt{|V_{SB} - \phi_o|})$ for p- and n-MOSFETs, respectively. The plot is obtained from the following MOSFET threshold voltage equation

$$V_T = V_{TO} + \gamma(\sqrt{|-\phi_o + V_{SB}|} - \sqrt{|\phi_o|}) \tag{B.3}$$

where the surface potential, $\phi_o = 2\phi_F$. The slope of the linear plots in Figs. B.4 and B.5 gives the body-effect coefficient (or body factor).

Table B.1 summarizes the measured model parameters on fabricated n- and p-MOSFETs and the corresponding parameters available through MOSIS. A close agreement is obtained. All model parameters could not be extracted due to practical limitations.

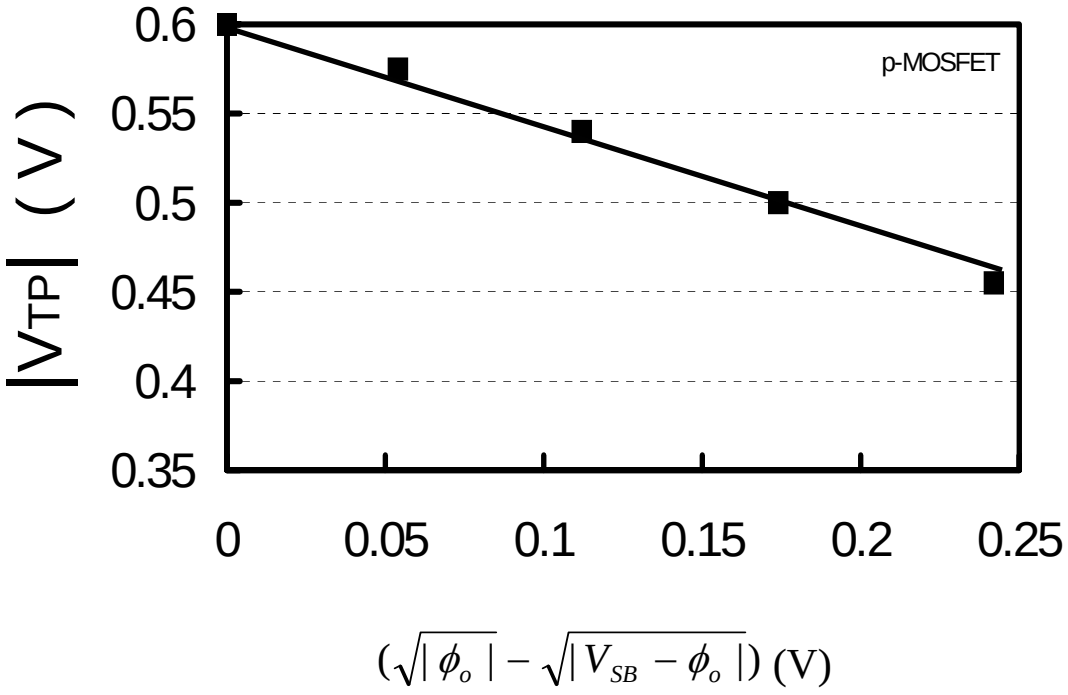

Figure B.4: V_T versus $(\sqrt{|\phi_o|} - \sqrt{|V_{SB} - \phi_o|})$ plot of a p-MOSFET.

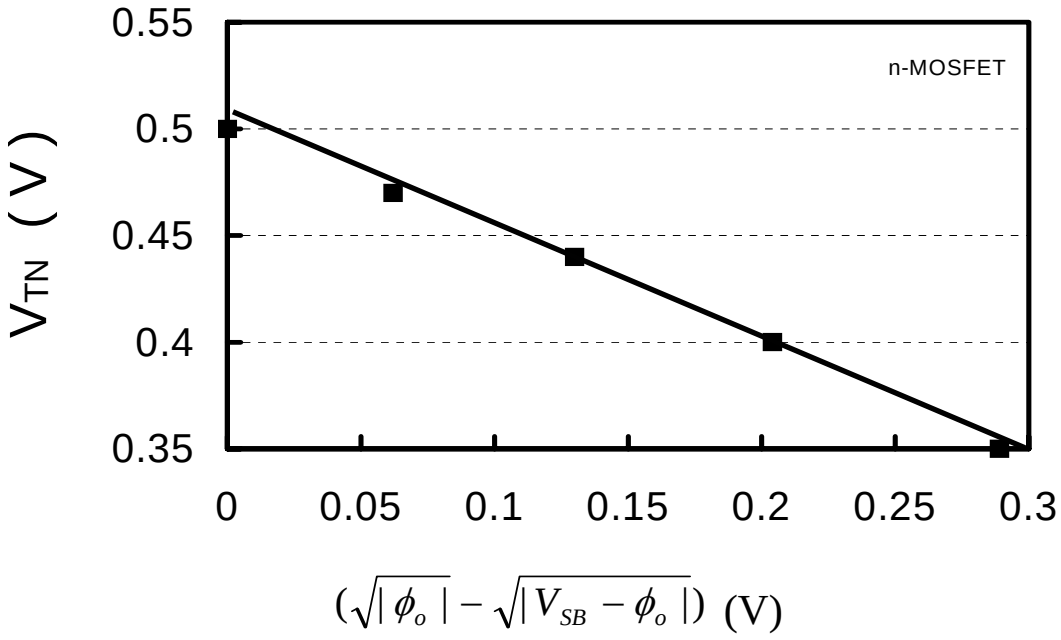

Figure B.5: V_T versus $(\sqrt{|\phi_o|} - \sqrt{|V_{SB} - \phi_o|})$ plot of an n-MOSFET.

Table B.1 A comparison of measured MOSFET model parameters with the MOSIS level 3 MOS model parameters.

Parameters	**n-MOSFET**		**p-MOSFET**	
	MOSIS	Extracted	MOSIS	Extracted
V_{TO}	0.56 V	0.50 V	0.79 V	0.60 V
$\frac{\mu C_{ox}}{2}$	$12.1\,\frac{\mu A}{V^2}$	$13.8\,\frac{\mu A}{V^2}$	$35.3\,\frac{\mu A}{V^2}$	$34.7\,\frac{\mu A}{V^2}$
ϕ_o	0.61 V	0.7 V	0.82 V	0.9 V
γ	$0.70\sqrt{V}$	$0.57\sqrt{V}$	$0.49\sqrt{V}$	$0.52\sqrt{V}$

APPENDIX C

MEASURMENT of AMPLIFIER PARAMETERS [35]

Figure C.1 shows a model of a non-ideal operational amplifier. C_{id} and R_{id} form the finite differential input impedance. The output resistance is modeled by R_{out}. The common mode input resistances are modeled by the resistor, R_{icm}. V_{OS} is the input offset voltage. I_{B1} and I_{B2} are the input bias currents. The common mode rejection ratio (CMRR) is modeled by the voltage controlled voltage source. The op-amp noise is modeled by two noise sources, the voltage noise generator, e_n^2 and the current noise generator, i_n^2. In the following sections, measurement techniques used in extraction of amplifies parameters are described.

C.1 Op-Amp Input Off-set Voltage (V_{OS}):

Input offset voltage is defined as the output off-set voltage divided by the gain of the amplifier when difference in the input voltage is zero. Figure C.2 shows the circuit configuration for measuring the input-offset voltage. In Fig. C.2, negative terminal of the amplifier is connected to the output in a unity gain configuration. Thus the input off-set voltage is transferred to the output of the amplifier which implies that the measured output voltage is equal to the measured input off-set voltage.

C.2 Common Mode Rejection Ratio (CMRR)

The CMRR is defined as follows:

$$CMRR = \frac{A_{dm}}{A_{cm}} \tag{C.1}$$

where A_{dm} and A_{cm} are pure differential mode gain and common mode gain, respectively. Figure C.3 shows the configuration for measuring the A_{cm}.

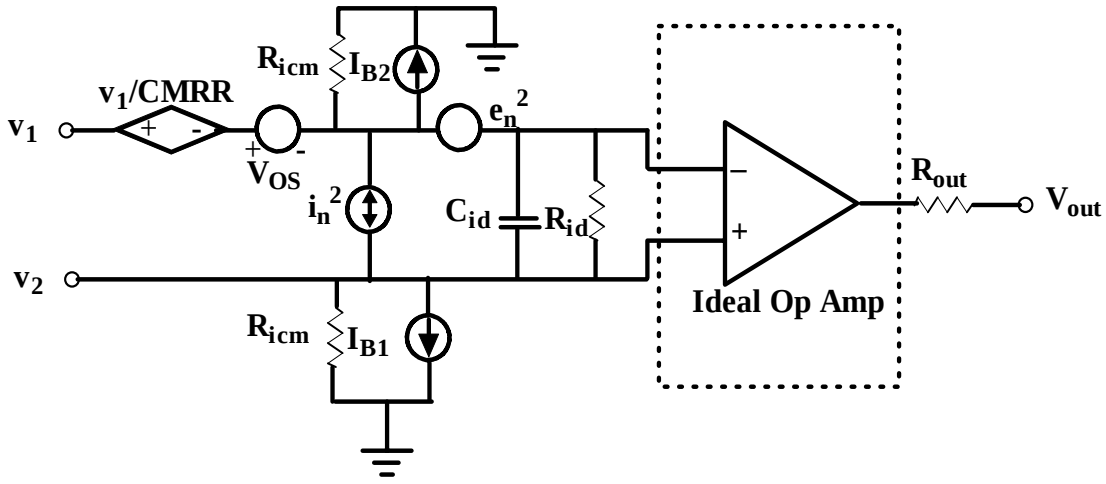

Figure C.1: A non-ideal operational amplifier.

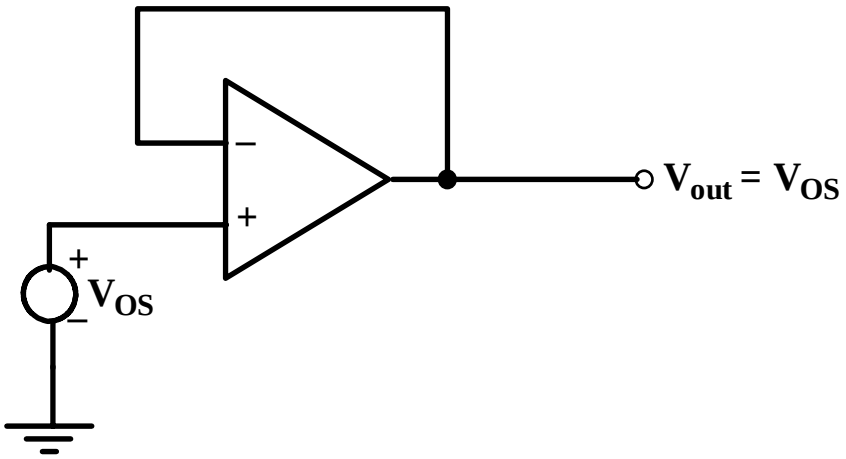

Figure C.2: The Input off-set voltage, V_{OS} measurement.

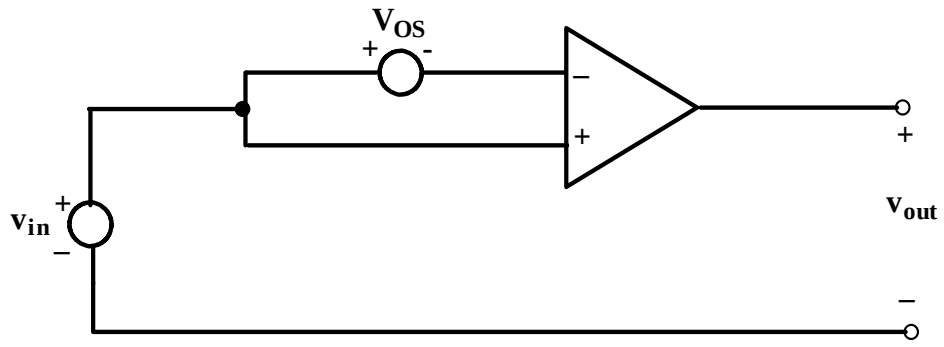

Figure C.3: The pure common mode gain, A_{cm} measurement.

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C.3 Power Supply Rejection Ratio (PSSR)

The power supply rejection ratio (PSSR) is defined as the product of open loop gain of the amplifier and ratio of the change in power supply divided by the change in the output voltage which is caused by the change in the power supply voltage. A small signal is inserted in series with the power supply voltage to measure PSRR as shown in Fig. C.4. PSSR can be calculated using the following equation:

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{out}} Av . \quad \text{(C.2)}$$

Eq. (C.2) can be re-written for the PSSR calculation for the amplifier in a unity gain configuration shown in Fig. C.4.

$$PSRR^{+} = \frac{v_{dd}}{v_{out}} \text{ and} \quad \text{(C.3)}$$

$$PSRR^{-} = \frac{v_{ss}}{v_{out}} . \quad \text{(C.4)}$$

C.4 Input Common-Mode Range (ICMR)

ICMR specifies the range of input common-mode voltage over which the differential amplifier continues to sense and amplify the difference signal with the same gain. Figure C.5 shows the ICMR measurement configuration where the amplifier is used in the unity-gain configuration. The ICMR is obtained from the linear past of the transfer curve, where the slope is unity, $v_{out}/v_{in} = 1$.

C.5 Slew Rate (SR)

Slew rate is defined as the rate of change of the output voltage. It is related to current sourcing or sinking capability of the amplifier. A unity gain configuration is used to measure the slew rate. With a square wave form input whose step is sufficiently large

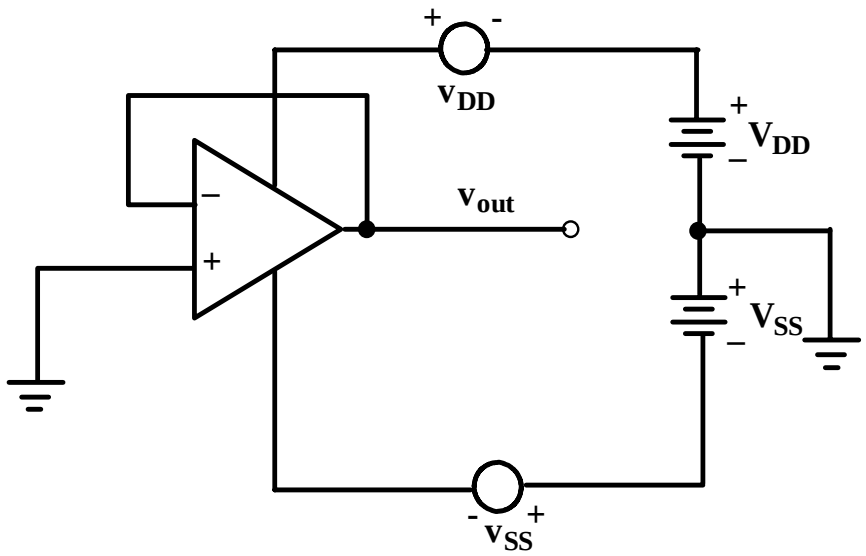

Figure C.4: PSRR measurement.

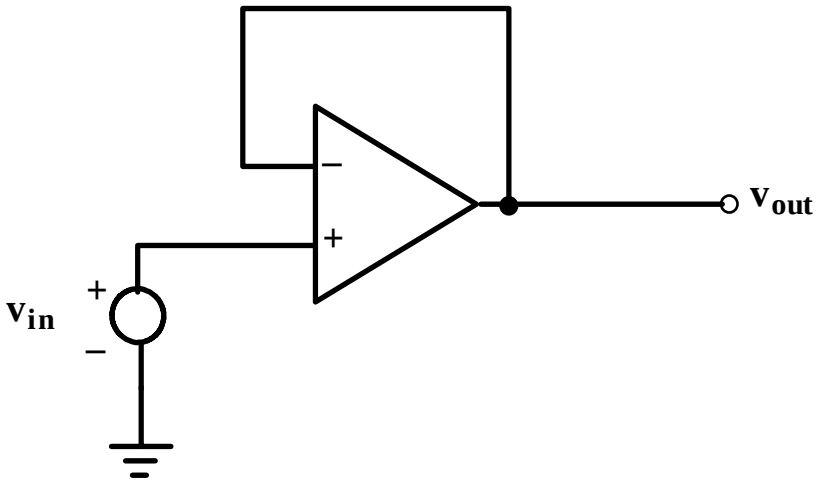

Figure C.5: ICMR measurement.

(> 0.5 V) is applied, the output of amplifier will slew since amplifier needs enough current to charge and discharge the load capacitor. The slew rate is determined by the slope of the output wave form. The slope of the rising output is SR^+. The slope of the falling output is SR^-. Figure C.6 shows the configuration of amplifier for measuring SR.

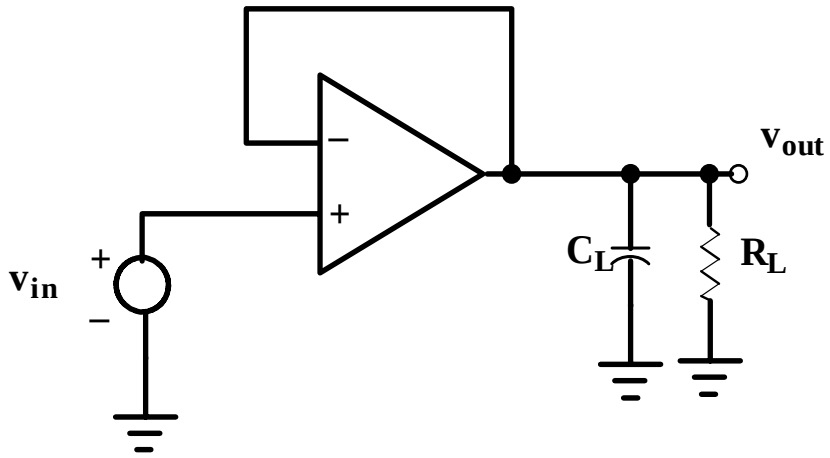

Figure C.6: Configuration of amplifier for measuring SR. R_L and C_L are included for the output loading during slew rate measurements.

APPENDIX D

LIST OF PUBLICATIONS

Journal Publications

C. Zhang, A. Srivastava and P. K. Ajmera "Low voltage CMOS Schmitt trigger circuits," *Electronics Letters*, Vol. 39, No. 24, pp. 1696-1698, 27th November 2003.

C. Zhang, A. Srivastava and P. K. Ajmera, "Noise analysis in a 0.8 V forward body-bias CMOS op-amp design," *Fluctuation and Noise Letters (FNL) – Special Issue on Noise in Devices and Circuits,* Vol. 4, No. 2, pp. L403-L412, June 2004.

Conference Publications

C. Zhang, A. Srivastava and P.K. Ajmera, "A 0.8 V ultra-low power CMOS operational amplifier design," *Proc. of 45th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. I 9-12, 2002, (Tulsa, Oklahoma, Aug. 4-7, 2002). 4th Best Student Paper Award among 10 best-selected papers in nearly 200 papers from 32 countries for the Student Paper Contest.

C. Zhang, T. Xin, A. Srivastava and P.K. Ajmera, "Ultra-low power CMOS operational amplifier for a neural microprobe," *Proc. of SPIE*, Vol. 5055, pp. 29-35, 2003, (San Diego, CA, 2-6 March 2003).

C. Zhang, A. Srivastava and P. K. Ajmera, "Noise analysis of an ultra-low power CMOS operational amplifier," *Proc. of SPIE – Fluctuations and Noise 2003: Noise in Devices and Circuits*, Vol. 5113, pp. 294-300, 2003, (Santa Fe, NM, 1-4 June 2003).

C. Zhang, A. Srivastava and P. K. Ajmera, "0.8 V ultra-low power CMOS analog multiplexer for remote biological and chemical signal processing," *Proc. of SPIE*, Vol. 5389, pp. 13-19, 2004 (San Diego, CA, 15-18 March 2004).

T. Xin, P.K. Ajmera, C. Zhang, A. Srivastava, "High-aspect ratio neural probes for monolithic integration with ultra-low-power CMOS operational amplifier circuit," *Proc. of SPIE*, Vol. 5389, pp. 20-25, 2004 (San Diego, CA, 15-18 March 2004).

C. Zhang, D. Ma and A. Srivastava, "Integrated adaptive DC/DC conversion with adaptive pulse-train technique for low-ripple fast response regulation," *Proc. of IEEE International Symposium on Low Power Electronics and Design (ISLPED'04)*, pp. 257-262, 2004 (Newport Beach, CA).

T. Xin, P. K. Ajmear, C. Zhang and A. Srivastava, "Post-CMOS chip-level processing for high-aspect ratio microprobe fabrication utilizing pulse plating," *Proc. of SPIE*, Vol. 5763, 2005, in press (San Diego, CA, 6-10 March 2005).

VITA

Chuang Zhang was born on February 25, 1974, in Beijing, China. He received his Bachelor of Science in physics from Tsinghua University, Beijing, China, in July 1997. He received his Master of Science in materials science from University of Southern California, Los Angeles, U.S.A., in August 1999. He has been enrolled in the Department of Electrical and Computer Engineering at Louisiana State University, Baton Rouge, Louisiana, since August 2000 to pursue his doctoral studies. His research interests include low power mixed-signal integrated circuits and noise in devices and circuits.